Hall Ticket Number :										

R11/R13

Code: 1G383

IV B.Tech. II Semester Supplementary Examinations December 2017

DSP Processors & Architectures

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer any ***five*** questions

All Questions carry equal marks (**14 Marks** each)

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1.	a)	Explain the architecture of typical VLIW processor in detail	7M
	b)	Explain the issues of pipelining in Programmable DSP's	7M
2.	a)	Write about block floating point format with example	7M
	b)	Explain about the sources of errors in DSP implementations because of fixed word length.	7M
3.	a)	Explain the concepts of hardware architectures and parallelism related to speed issues required for programmable DSP devices.	7M
	b)	Draw and explain the block diagram of a barrel shifter and present the implementation of a 4-bit shift-right barrel shifter	7M
4.	a)	Describe the multiplier/adder unit of TMS320c54xx processor with a neat block diagram.	7M
	b)	Describe any four data addressing modes of TMS320c54xx processor.	7M
5.	a)	Implement the interpolation filters using basic DSP algorithms	7M
	b)	Implement the PID controller using the relevant DSP algorithm.	7M
6.	a)	Implement an 8-point FFT on the TMS320C54XX processor with the required FFT algorithm.	7M
	b)	Write notes on butterfly computation in connection with FFT algorithms.	7M
7.	a)	Explain a CODEC interface circuit with its programming and an example.	7M
	b)	Write notes on McBSP programming	7M
8.	a)	Compare the performance of the systems designed using FPGAs and digital signals processors.	7M
	b)	Explain the design flow for an FPGA based system design.	7M

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