Hall Ticket Number :										

R11/R13

Code: 1G383

IV B.Tech. II Semester Supplementary Examinations September 2020

DSP Processors and Architectures

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer any ***five*** questions

All Questions carry equal marks (**14 Marks** each)

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1.	a)	Explain the architecture of typical VLIW processor in detail	7M
	b)	Explain the issues of pipelining in Programmable DSP's	7M
2.	a)	Discuss about the errors that occur during the conversion of an analog signal to digital signal?	8M
	b)	Describe dynamic range and precision in DSP systems?	6M
3.	a)	Explain data addressing capabilities of programmable DSPs?	6M
	b)	List out the speed issues in P-DSPs? Explain in detail?	8M
4.	a)	Describe the multiplier/adder unit of TMS320c54xx processor with a neat block diagram.	6M
	b)	Describe any four data addressing modes of TMS320c54xx processor.	8M
5.	a)	Define Q-notation and illustrate the concept of numbers represented using Q-notation?	6M
	b)	Discuss about 2D signal processing and decimation filters?	8M
6.	a)	Determine the optimum scaling factor for the DIT-FFT butterfly? Justify How scaling prevents the overflow conditions in butterfly computations?	10M
	b)	Explain how bit-reversed index-generation is implemented in TMS320C54XX DSP?	4M
7.	a)	Explain a CODEC interface circuit with its programming and an example.	8M
	b)	Write notes on McBSP programming	6M
8.	a)	Discuss about the CAD tools for FPGA based system design?	8M
	b)	Describe the overview of Open Multimedia Applications Platform?	6M

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