Hall Ticket Number :										

R11

Code: 1G383

IV B.Tech. II Semester Supplementary Examinations Nov/Dec 2019

DSP Processors and Architectures

(Electronics & Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *any five* questions

All Questions carry equal marks (14 Marks each)

****

1. a) Explain the difference between a MAC instruction and MAC with data shift instruction. When the latter instruction is preferred. 7M

   b) Distinguish between the synchronous and asynchronous mode of operation of serial ports. 7M

2. a) Show that the dynamic range of a signal increases by 6dB for each additional bit used to represent its value. 7M

   b) Compute the dynamic range and the percentage resolution for a block floating-point with a 4-bit exponent used in a 16-bit fixed-point processor 7M

3. a) With a neat block diagram explain about address generation unit of a DSP processor? 6M

   b) Illustrate the following special addressing modes :
      i) Bit reversed addressing mode
      ii) Circular addressing mode 8M

4. Draw and explain the architecture of TMS320C54XX processor? 14M

5. Develop a decimation filter program that can be used to decimate by a factor of 2^5 using a subroutine to decimate by a factor of 2 in conjugation with appropriate filters. 14M

6. Develop a TMS320C54xx subroutine to multiply two 3 x 3 matrices 14M

7. a) How to handle interrupts? Explain with the help of a flowchart? 7M

   b) Draw the circuit for interfacing ADC and DAC to TMS320C54XX processor and explain? 7M

8. Explain the functional block diagram of Xilinx XC4000E family CLB with neat diagram 14M

***