Hall Ticket Number :										

R-11 / R-13

Code: 1G383

IV B.Tech. II Semester Supplementary Examinations October 2020

DSP Processors & Architectures

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer any **five** questions

All Questions carry equal marks (**14 Marks** each)

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1.	a)	Explain the architecture of typical VLIW processor in detail	7M
	b)	Explain the issues of pipelining in Programmable DSP's	7M
2.	a)	Explain about the floating-point format for signals and coefficients in DSP systems.	7M
	b)	Discuss in brief about DSP computational errors in DSP implementation.	7M
3.	a)	Explain the concepts of hardware architectures and parallelism related to speed issues required for programmable DSP devices.	7M
	b)	Draw and explain the block diagram of a barrel shifter and present the implementation of a 4-bit shift-right barrel shifter	7M
4.	a)	Explain any four addressing modes supported by TMS320C54xx processors.	7M
	b)	Write a brief note on interrupts of TMS320C54xx processors.	7M
5.	a)	Write an algorithm to implement interpolation filter on a DSP.	7M
	b)	Implement DSP algorithm for PID controller.	7M
6.		Implement an FFT algorithm for a bit-reversal index algorithm.	14M
7.	a)	Explain a CODEC interface circuit with its programming and an example.	7M
	b)	Write notes on McBSP programming	7M
8.	a)	Compare the performance of the systems designed using FPGAs and digital signals processors.	7M
	b)	Explain the design flow for an FPGA based system design.	7M

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