Hall Ticket Number :										

R-14

Code: 4PA312

M.Tech. I Semester Regular & Supplementary Examinations January 2017

Advanced Digital Signal Processing

(DECS)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) Define and Classify Discrete Time Systems. Check whether the following is a Linear, Casual system or not Y[n]= 4 X[n]+8 X[n-1]. 6M

   b) State and Prove any Two properties of CTFT 6M

OR

2. a) Derive Complementary Transfer Function of LTI Discrete-Time System. 6M

   b) Briefly write about the following

   i) Digital Two Pairs ii) Band Limited Discrete Time Signal 6M

UNIT–II

3. a) Describe in detail about the design of IIR filter using Least Square Design method 6M

   b) With an example explain the Tunable IIR Digital filter. 6M

OR

4. a) Explain the design of an IIR filter using Pade approximation method 6M

   b) Differentiate between IIR and FIR filters. 6M

UNIT–III

5 Design and Draw the Flow Graph for Computation of DFT with **N=12** by using the following algorithms

i) Cooley Tuckey Method ii) Prime Factor algorithm 12M

OR

6. a) Explain in detail about Computation of DFT using Chirp Z-Transform 6M

   b) Discuss about fast DFT algorithm based on index mapping 6M

UNIT–IV

7. Design and explain the following methods for Power Spectrum Estimation

   i) Weltch Method
   ii) Burg Method
   iii) Bartlett Method 12M

OR

8. a) Write a short note on the parametric spectrum estimation techniques. 6M

   b) Compare the nonparametric power spectrum estimation techniques. 6M

UNIT–V

9 a) Briefly Discuss about Decimator for sampling Rate conversion 6M

   b) Draw and explain the structure of Direct-form realization of FIR filter in sampling rate conversion by factor I/D. 6M

OR

10 a) Explain in detail about Sampling Rate Conversion by a rational factor I/D 6M

   b) Discuss about Oversampling A/D converter. 6M

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Hall Ticket Number :										

R14

Code: 4PA313

M.Tech. I Semester Regular & Supplementary Examinations January 2017

Digital Communication Techniques

(DECS)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1.	a)	Explain about i) Markov Chains ii) Circular Random Processes	8M
	b)	Summarize on the different Signal space Concepts.	4M

OR

2.	a)	Discuss and plot the probability density functions of Gaussian, Rayleigh and Rician distributions.	4M
	b)	Classify and explain the different types of Random Processes	8M

UNIT–II

3.		Describe the Implementation an Optimum Receiver for AWGN Channel	12M

OR

4.		Explain about Phase and Quadrature Amplitude Modulation in detail.	12M

UNIT–III

5.	a)	Illustrate the concept of Multi dimensional signaling.	7M
	b)	Sketch and explain the block diagram of Generalized RAKE demodulator.	5M

OR

6.		Explain how frequency-selective channel can be modeled by using Tapped-Delay model.	12M

UNIT–IV

7.		Discuss in detail about the Nyquist Criterion for design of Band-Limited Signals to avoid Inter symbol Interference (ISI).	12M

OR

8.	a)	Outline the concept of Linear Equalization.	3M
	b)	Describe how Mean-Square-Error (MSE) criterion can used for optimization of Equalizer co-efficients.	9M

UNIT–V

9.	9	Explain the concept of Modulation and Demodulation in an OFDM System.	12M

OR

10.	a)	What is the role of cyclic Prefix appending to reduce Inter Symbol Interferance.	4M
	b)	Sketch and explain the block diagram of Filter bank implementation of OFDM receiver.	8M

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Hall Ticket Number :										

R14

Code: 4PA311

M.Tech. I Semester Regular & Supplementary Examinations January 2017

Digital System Design

(D E C S)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) Explain how ROMs and PLAs are used in designing sequential circuits 6M

   b) Explain how does the ASM chart differ from a software flow chart? 6M

OR

2. a) Implement the logic function 'F' using ROM
   F = A'BC' + A'BC + AB'C + ABC 6M

   b) Draw an ASM chart of JK flip-flop. Realize it using SR flip flop and required gates 6M

UNIT–II

3. a) Explain how signature analysis is used for testing bridging faults? 6M

   b) Describe the algorithmic steps involved in PODEM. 6M

OR

4. a) With an example, explain the transition count testing method. 6M

   b) What is the significance of Kohavi Algorithm? Explain how it detects multiple faults in a two-level networks with a simple example 6M

UNIT–III

5. An unknown three state machine with two input symbols 0 and 1 is provided with the input sequence X, and it responds by producing the output sequence Z, as shown below:

x	1	1	0	0	1	0	1	0	1	1	1	1	1	0	0	0	1	1	0	0	1	0	1
y	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	1	1	0	0	0

   Show that this experiment is sufficient to identify the machine uniquely. 12M

OR

6. a) Explain design of fault detection experiment 6M

   b) Explain the concept of Machine identification with an example 6M

UNIT–IV

7. a) Describe the advantages of PLA minimization and folding. 6M

   b) Design a 3 bit BCD to grey code converter and realize the circuit using PLA and then show that how folding will reduce the number of cross points given on the PLA. 6M

OR

8. Discuss in detail about the types of faults in PLA with example. 12M

UNIT–V

9. a) Explain the following with examples:
   (i) Flow table (ii) State reduction. 6M

   b) With respect to an asynchronous sequential machine, explain about minimal closed covers. 6M

OR

10. a) Write note on minimum closed covers and hazards 6M

    b) Explain races and cycles in sequential circuits. 6M

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Hall Ticket Number :										

R14

Code: 4PB311

M.Tech. I Semester Regular & Supplementary Examinations January 2017

Embedded System Concepts

(Common to DECS, Embedded Systems, VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) What is meant by Embedded system? with a suitable example, Explain soft and hard embedded systems 8M

   b) What are the challenges in design of an Embedded system? 4M

OR

2. a) With a suitable diagrams ,Explain architecture of kernel 6M

   b) What you mean by System-on-Chip(SoC)? How will the definition of an embedded system change with a SoC? 6M

UNIT–II

3. a) Discuss about various memories used in Embedded systems. 6M

   b) What are the parameters taken into account for the selection of a processor for designing embedded systems? 6M

OR

4. a) Describe the role of RAM in embedded systems? 6M

   b) What is the necessity of DMA? Explain operation of it. 6M

UNIT–III

5. a) Explain architecture of IEEE -488 bus 8M

   b) Difference between OS and RTOS? 4M

OR

6. a) Explain Round Robin and function Queue scheduling algorithms 8M

   b) Explain architecture of RS-232 Serial bus 4M

UNIT–IV

7. a) Discuss various steps involved in the development phase of an Embedded system. 8M

   b) What are the issues in the design of an Embedded system? 4M

OR

8. Explain software and Hard ware tools for design of an Embedded system. 12M

UNIT–V

9. Describe the design aspects of smart cards 12M

OR

10. With a suitable diagrams, explain the design issues of Automatic Chocolate vending Machine 12M

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Hall Ticket Number :										

R14

Code: 4PC314

M.Tech. I Semester Regular & Supplementary Examinations January 2017

Modelling & Synthesis through Verilog HDL

(Common to DECS & VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) List the operands and expressions used in Verilog. 6M

   b) Construct a 2 i/p NOR gate using behaviour model Verilog code. Also write the test bench for the above program. 6M

OR

2. Elaborate the various Data Types and Strings used in Verilog with suitable examples. 12M

UNIT–II

3. a) Write briefly about the Propagation Delay using built-in constructs. 4M

   b) Design a 2-to-1 multiplexer by using UDP. The select signal is S, inputs arei0, i1, and the output is Out. If the select signal S = x, the output Out is always 0. If S = 0, then out = i0. If S = 1, then out = i1. 8M

OR

4. a) Discuss briefly about Initialization of Sequential Primitives. 6M

   b) Write short notes on the effects of Inertial Delay. 6M

UNIT–III

5. a) Write Verilog program for 2 input CMOS NOR gate using switch level model 6M

   b) What are ambiguous signals? Explain briefly. 6M

OR

6. a) Explain in detail the Bi-Directional Switches, its importance with a suitable example. 6M

   b) What is Procedural Assignment? Write a sample program using Procedural Continuous Assignments and Procedural Timing Controls. 6M

UNIT–IV

7. Explain the importance of the Don't cares, Tri-State outputs and the Tri-state Buffers? 12M

OR

8. Discuss in detail about the Horizontal and Vertical partitioning in Digital Design with example. 12M

UNIT–V

9. a) Discuss briefly about the synthesis of Nets. 6M

   b) Write briefly about the synthesis of Register variables. 6M

OR

10. Explain in detail the synthesis of Multi-cycle operations? 12M

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Hall Ticket Number :										

R14

Code: 4PA314

M.Tech. I Semester Regular & Supplementary Examinations January 2017

Wireless Communications

(DECS)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) Explain the evolution of the Mobile Radio Communications 6M
   b) Explain how Personal Area Network (PAN) provided by Bluetooth Standard 6M

OR

2. a) Explain different types of WLL Techniques in detail. 6M
   b) Compare between 3G W-CDMA, 3D cdma2000 and 3G TD-SCDMA Standards 6M

UNIT–II

3 a) Define Brewster Angle and derive the expression for the same 5M
   b) With a neat diagram explain in detail Single Knife-edge and Multiple Knife-edge Diffraction model 7M

OR

4 a) Illustrate the Impulse Response Model of a Multipath Channel 6M
   b) With neat diagram explain Direct RF Pulse System 6M

UNIT–III

5 a) Derive Selection Diversity Improvement 6M
   b) Assume five branch diversity is used, where each branch receives an independent Rayleigh fading signal. If the average SNR is 20 dB, determine the probability that the SNR will drop below 10 dB. Compute the mean SNR. Compare this with the case of a single receiver without diversity. 6M

OR

6 With neat diagram explain in detail Direct Sequence Spread Spectrum (DS-SS) transmitter and receiver 12M

UNIT–IV

7 a) List the features of FDMA in detail. Explain the Nonlinear Effects in FDMA 8M
   b) In US AMPS, 416 channels are allocated to various cellular operators. The channel between them is 30 kHz with the guard band of 10 kHz. Calculate the spectrum allocation given to each operator 4M

OR

8 a) Evaluate the Capacity of Cellular CDMA 6M
   b) In IS-95 CDMA system, if W = 1.25 MHz, R = 9600 bps, and N = 14 users
   (a) Calculate E_b/N_o (b) When no voice activity is there, calculate E_b/N_o for omnidirectional antennas (c) If voice quality = 3/8 and three sector antennas are used, calculate the total number of users' cell 6M

UNIT–V

9 Evaluate the Capacity of frequency selective fading channels 12M

OR

10 Illustrate Narrow Band MIMO model in detail 12M

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