Hall Ticket Number :										

R14

Code: 4PC313

M.Tech. I Semester Regular & Supplementary Examinations January 2017

Digital IC Design

(Common to Embedded Systems and VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1 Evaluating the robustness of the CMOS Inverter and analyze its Static behavior. 12M

OR

2 What is the Power, Energy and Energy-Delay of CMOS Inverter? 12M

UNIT–II

3 Explain Static CMOS designing of combinational logic gates. 12M

OR

4 Explain the pipelining technique for optimization of sequential circuits. 12M

UNIT–III

5 What is the impact of Technology scaling on CMOS Inverter metrics? 12M

OR

6 Explain the low power design techniques of voltage scaling, switching activity and reduced capacitance in CMOS circuit. 12M

UNIT–IV

7 What is the basic need of design rules? Explain CMOS design rules. 12M

OR

8 Explain the effects of sheet resistances and various capacitances on CMOS designs. 12M

UNIT–V

9 Design a modified Booth's multiplier. 12M

OR

10 Explain the power dissipation occurred in CMOS memories. 12M

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R14

Code: 4PB311

M.Tech. I Semester Regular & Supplementary Examinations January 2017

Embedded System Concepts

(Common to DECS, Embedded Systems, VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) What is meant by Embedded system? with a suitable example, Explain soft and hard embedded systems 8M

   b) What are the challenges in design of an Embedded system? 4M

OR

2. a) With a suitable diagrams ,Explain architecture of kernel 6M

   b) What you mean by System-on-Chip(SoC)? How will the definition of an embedded system change with a SoC? 6M

UNIT–II

3. a) Discuss about various memories used in Embedded systems. 6M

   b) What are the parameters taken into account for the selection of a processor for designing embedded systems? 6M

OR

4. a) Describe the role of RAM in embedded systems? 6M

   b) What is the necessity of DMA? Explain operation of it. 6M

UNIT–III

5. a) Explain architecture of IEEE -488 bus 8M

   b) Difference between OS and RTOS? 4M

OR

6. a) Explain Round Robin and function Queue scheduling algorithms 8M

   b) Explain architecture of RS-232 Serial bus 4M

UNIT–IV

7. a) Discuss various steps involved in the development phase of an Embedded system. 8M

   b) What are the issues in the design of an Embedded system? 4M

OR

8. Explain software and Hard ware tools for design of an Embedded system. 12M

UNIT–V

9. Describe the design aspects of smart cards 12M

OR

10. With a suitable diagrams, explain the design issues of Automatic Chocolate vending Machine 12M

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Hall Ticket Number :										

R14

Code: 4PC315

M.Tech. I Semester Regular & Supplementary Examinations January 2017

FPGA Architectures and Applications

(Common to VLSISD and Embedded Systems)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) What are the features of ROM, PLD, PAL devices? Mention some of their applications.
   b) With the help of sketches describe the Cypres FALSH 370 Device Technology.

OR

2. a) Explain about Altera's – Max 5000/7000 Series CPLDs.
   b) Describe the Architecture of Lattice PLSI's –3000series.

UNIT–II

3. a) Describe the Programming technologies of a general FPGA.
   b) Explain about Routing Architecture of FPGAs.

OR

4. a) Give the design flow and Technology mapping for any general FPGA.
   b) Draw and explain the simplified block diagram of CLB of a generalized FPGA.

UNIT–III

5. a) With a neat schematic, give the architecture of Xylinx 4000 FPGA.
   b) Explain the architecture of ACTEL's ACT-1,2,3 and their Speed Performance.

OR

6. a) Compare Alteras' Flex 8000 and 10000 series FPGAs
   b) Explain about the AT & T's – ORCA (Optimized Reconfigurable Cell Array)

UNIT–IV

7. a) Explain about the Top Down design approach of a state machine.
   b) Explain how realization of state machine chart using PAL is done.

OR

8. a) Explain the Basic Concepts and Properties of Petrinetes for State Machines.
   b) Explain the implementation of Traffic Light Controller using Finite State Machine.

UNIT–V

9. a) Give an example and explain for a system design of Architectures Centered around non-registered PLDS.
   b) Describe the use of ASMs in One – Hot Design.

OR

10. a) Explain the System Level Design of a parallel Controller.
    b) Explain the System Level Design of One – Hot Method.

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Hall Ticket Number :										

R14

Code: 4PB312

M.Tech. I Semester Regular & Supplementary Examinations January 2017

Micro Controllers & Interfacing

(Embedded Systems)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) How microcontrollers differ from microprocessors 4M
   b) Explain the internal memory architecture of 8051 8M

OR

2. a) Explain different modes of timer. 6M
   b) Generate a square wave of 10KHZ square wave on P0.4 pin using timer. 6M

UNIT–II

3. a) Design the circuit to interface Array of LEDs one after another with delay. 6M
   b) Give the structure of Keyboard cum Display Controller (8279) interfacing. 6M

OR

4. a) Discuss the Analog input interfacing. 6M
   b) Explain Prototype MCU based measuring instruments 6M

UNIT–III

5. a) Explain the Motorola 68HC11 Architecture 8M
   b) List Analog to digital conversion features. 4M

OR

6. a) Explain Interrupts in Motorola 68HC11 6M
   b) Discuss Output compare module with diagram 6M

UNIT–IV

7. a) Discuss memory structure in PIC controllers 6M
   b) Explain Register file structure 6M

OR

8. a) Discuss the structure of I/O ports. 8M
   b) List the functions serial peripheral interface 4M

UNIT–V

9. a) List the advantages of RISC machines 4M
   b) Explain architecture of ARM controller with suitable sketch 8M

OR

10. a) List different registers visible in different states 6M
    b) Differentiate ARM and THUMB instruction set 6M

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R14

Code: 4PB313

M.Tech. I Semester Regular & Supplementary Examinations January 2017

Real Time Operating Systems

(Embedded Systems)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) Distinguish semaphore and mutex 6M

   b) If the process time is stored as a signed 32-bit integer, and if the system counts 100 ticks per second, after how many days will the value overflow? 6M

OR

2. a) Demonstrate Pipes, Message Queues and shared memory with suitable example 8M

   b) Explain in detail various input/output file commands 4M

UNIT–II

3. a) What is meant by release times, deadlines, and timing constraints in real time systems? 6M

   b) Illustrate the reasons for requiring timing guarantees in real time systems. 6M

OR

4. Examine temporal parameters of real time work load in real time systems 12M

UNIT–III

5. a) Demonstrate Clock-Driven approach with example 6M

   b) Explain Priority –Driven approach with example 6M

OR

6. Explain Off-line and On-line scheduling in detail 12M

UNIT–IV

7. a) What are the various functionalities of operating system? 6M

   b) What are the capabilities of commercial operating system 6M

OR

8. What are the various hand held operating systems? Explain in detail with examples 12M

UNIT–V

9. a) What are the various types of faults? Explain the temporal behavior and output behavior classification. 8M

   b) Explain fault and error containment in detail 4M

OR

10. a). What is meant by sift out redundancy? 6M

    b) Explain software redundancy with example 6M

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R-14

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M.Tech. I Semester Regular & Supplementary Examinations January 2017

VLSI Technology

(Common to Embedded Systems & VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) Explain how gm & gds are depend on fabrication parameters 6M
   b) Determine Z_{PU}/Z_{PD} for an NMOS inverter Driven by another NMOS inverter 6M

OR

2. a) Compare between CMOS Technology and BiCMOS Technology 6M
   b) Explain about the latch–up in CMOS Circuits 6M

UNIT–II

3. a) Draw and explain the stick diagram of CMOS three input NAND gate 6M
   b) Explain about the Design rules and Process parameters 6M

OR

4. a) What are the wires and vias and how to construct them? 6M
   b) Explain about layout design tools 6M

UNIT–III

5. a) Design the static complementary pullup and pull down network for the logic expression (a+b)(c+d) 6M
   b) Explain about the domino logic 6M

OR

6. a) Explain the delay through inductive interconnect 6M
   b) Explain about alternate gate Circuits 6M

UNIT–IV

7. a) Explain about switched logic networks with an example 6M
   b) Explain about power optimization 6M

OR

8. a) Explain the terms controllability and absevability related to combinational network testing with an example 6M
   b) Explain about simulation with an example 6M

UNIT–V

9. a) What is one-phase and two-phase clocking systems? Compare them 6M
   b) Explain about design validation and testing 6M

OR

10. a) Explain system-on-chip concept using platform based design 6M
    b) Explain about off–chip Connections 6M

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