Hall Ticket Number :										

R14

Code: 4PC312

M.Tech. I Semester Regular & Supplementary Examinations January 2017

Analog IC Design

(VLSI System Design)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) Draw the circuit of a Source flower with current mirror to supply bias current and obtain the expression for gain and output impedance. 6M

   b) Write short notes on Source- Degenerated current mirrors 6M

OR

2. a) Deduce the small signal model for an n-channel MOSFET taking into account the body effect. 6M

   b) Explain common source amplifier with current mirror active load. 6M

UNIT–II

3. a) Explain about Folded cascade op amp 8M

   b) Deduce the necessary condition that ensures zero input-offset voltage for a two stage op amp. 4M

OR

4. Draw the circuit of Current feedback operational amplifier and derive an expression for gain and slew rate 12M

UNIT–III

5. a) Explain the operation of switched capacitor gain circuit. 6M

   b) Explain about Biquad filters. 6M

OR

6. a) Compare and contrast CMOS and BICMOS sample and hold circuits and their performances 6M

   b) What is a switched capacitor filter? List important features of it. How does it differ from analog filter? 6M

UNIT–IV

7. a) Draw and explain the Nyquist rate D/A converter using binary scaled converter. 6M

   b) Explain successive approximation A/D converter with a neat circuit diagram 6M

OR

8. a) Discuss about the following A/D Converters
      i. Two Step Converter.
      ii. Pipelined converter 8M

   b) Compare different types of A/D Converters 4M

UNIT–V

9. a) Discuss in detail the noise shaped delta sigma modulator 6M

   b) Derive the component values of 1st order continuous time filter 6M

OR

10. a) Write brief notes on second order Bandpass oversampling modulator. 6M

    b) Draw block diagram of oversampling converter without noise shaping and explain 6M

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Hall Ticket Number :										

R14

Code: 4PC313

M.Tech. I Semester Regular & Supplementary Examinations January 2017

Digital IC Design

(Common to Embedded Systems and VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1 Evaluating the robustness of the CMOS Inverter and analyze its Static behavior. 12M

OR

2 What is the Power, Energy and Energy-Delay of CMOS Inverter? 12M

UNIT–II

3 Explain Static CMOS designing of combinational logic gates. 12M

OR

4 Explain the pipelining technique for optimization of sequential circuits. 12M

UNIT–III

5 What is the impact of Technology scaling on CMOS Inverter metrics? 12M

OR

6 Explain the low power design techniques of voltage scaling, switching activity and reduced capacitance in CMOS circuit. 12M

UNIT–IV

7 What is the basic need of design rules? Explain CMOS design rules. 12M

OR

8 Explain the effects of sheet resistances and various capacitances on CMOS designs. 12M

UNIT–V

9 Design a modified Booth's multiplier. 12M

OR

10 Explain the power dissipation occurred in CMOS memories. 12M

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Hall Ticket Number :										

R14

Code: 4PB311

M.Tech. I Semester Regular & Supplementary Examinations January 2017

Embedded System Concepts

(Common to DECS, Embedded Systems, VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) What is meant by Embedded system? with a suitable example, Explain soft and hard embedded systems 8M

   b) What are the challenges in design of an Embedded system? 4M

OR

2. a) With a suitable diagrams ,Explain architecture of kernel 6M

   b) What you mean by System-on-Chip(SoC)? How will the definition of an embedded system change with a SoC? 6M

UNIT–II

3. a) Discuss about various memories used in Embedded systems. 6M

   b) What are the parameters taken into account for the selection of a processor for designing embedded systems? 6M

OR

4. a) Describe the role of RAM in embedded systems? 6M

   b) What is the necessity of DMA? Explain operation of it. 6M

UNIT–III

5. a) Explain architecture of IEEE -488 bus 8M

   b) Difference between OS and RTOS? 4M

OR

6. a) Explain Round Robin and function Queue scheduling algorithms 8M

   b) Explain architecture of RS-232 Serial bus 4M

UNIT–IV

7. a) Discuss various steps involved in the development phase of an Embedded system. 8M

   b) What are the issues in the design of an Embedded system? 4M

OR

8. Explain software and Hard ware tools for design of an Embedded system. 12M

UNIT–V

9. Describe the design aspects of smart cards 12M

OR

10. With a suitable diagrams, explain the design issues of Automatic Chocolate vending Machine 12M

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Hall Ticket Number :										

R14

Code: 4PC315

M.Tech. I Semester Regular & Supplementary Examinations January 2017

FPGA Architectures and Applications

(Common to VLSISD and Embedded Systems)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) What are the features of ROM, PLD, PAL devices? Mention some of their applications.
   b) With the help of sketches describe the Cypres FALSH 370 Device Technology.

OR

2. a) Explain about Altera's – Max 5000/7000 Series CPLDs.
   b) Describe the Architecture of Lattice PLSI's –3000series.

UNIT–II

3. a) Describe the Programming technologies of a general FPGA.
   b) Explain about Routing Architecture of FPGAs.

OR

4. a) Give the design flow and Technology mapping for any general FPGA.
   b) Draw and explain the simplified block diagram of CLB of a generalized FPGA.

UNIT–III

5. a) With a neat schematic, give the architecture of Xylinx 4000 FPGA.
   b) Explain the architecture of ACTEL's ACT-1,2,3 and their Speed Performance.

OR

6. a) Compare Alteras' Flex 8000 and 10000 series FPGAs
   b) Explain about the AT & T's – ORCA (Optimized Reconfigurable Cell Array)

UNIT–IV

7. a) Explain about the Top Down design approach of a state machine.
   b) Explain how realization of state machine chart using PAL is done.

OR

8. a) Explain the Basic Concepts and Properties of Petrinetes for State Machines.
   b) Explain the implementation of Traffic Light Controller using Finite State Machine.

UNIT–V

9. a) Give an example and explain for a system design of Architectures Centered around non-registered PLDS.
   b) Describe the use of ASMs in One – Hot Design.

OR

10. a) Explain the System Level Design of a parallel Controller.
    b) Explain the System Level Design of One – Hot Method.

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Hall Ticket Number :										

R14

Code: 4PC314

M.Tech. I Semester Regular & Supplementary Examinations January 2017

Modelling & Synthesis through Verilog HDL

(Common to DECS & VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) List the operands and expressions used in Verilog. 6M

   b) Construct a 2 i/p NOR gate using behaviour model Verilog code. Also write the test bench for the above program. 6M

OR

2. Elaborate the various Data Types and Strings used in Verilog with suitable examples. 12M

UNIT–II

3. a) Write briefly about the Propagation Delay using built-in constructs. 4M

   b) Design a 2-to-1 multiplexer by using UDP. The select signal is S, inputs arei0, i1, and the output is Out. If the select signal S = x, the output Out is always 0. If S = 0, then out = i0. If S = 1, then out = i1. 8M

OR

4. a) Discuss briefly about Initialization of Sequential Primitives. 6M

   b) Write short notes on the effects of Inertial Delay. 6M

UNIT–III

5. a) Write Verilog program for 2 input CMOS NOR gate using switch level model 6M

   b) What are ambiguous signals? Explain briefly. 6M

OR

6. a) Explain in detail the Bi-Directional Switches, its importance with a suitable example. 6M

   b) What is Procedural Assignment? Write a sample program using Procedural Continuous Assignments and Procedural Timing Controls. 6M

UNIT–IV

7. Explain the importance of the Don't cares, Tri-State outputs and the Tri-state Buffers? 12M

OR

8. Discuss in detail about the Horizontal and Vertical partitioning in Digital Design with example. 12M

UNIT–V

9. a) Discuss briefly about the synthesis of Nets. 6M

   b) Write briefly about the synthesis of Register variables. 6M

OR

10. Explain in detail the synthesis of Multi-cycle operations? 12M

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Hall Ticket Number :										

R-14

Code: 4PC311

M.Tech. I Semester Regular & Supplementary Examinations January 2017

VLSI Technology

(Common to Embedded Systems & VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) Explain how gm & gds are depend on fabrication parameters 6M
   b) Determine Z_{PU}/Z_{PD} for an NMOS inverter Driven by another NMOS inverter 6M

OR

2. a) Compare between CMOS Technology and BiCMOS Technology 6M
   b) Explain about the latch–up in CMOS Circuits 6M

UNIT–II

3. a) Draw and explain the stick diagram of CMOS three input NAND gate 6M
   b) Explain about the Design rules and Process parameters 6M

OR

4. a) What are the wires and vias and how to construct them? 6M
   b) Explain about layout design tools 6M

UNIT–III

5. a) Design the static complementary pullup and pull down network for the logic expression (a+b)(c+d) 6M
   b) Explain about the domino logic 6M

OR

6. a) Explain the delay through inductive interconnect 6M
   b) Explain about alternate gate Circuits 6M

UNIT–IV

7. a) Explain about switched logic networks with an example 6M
   b) Explain about power optimization 6M

OR

8. a) Explain the terms controllability and absevability related to combinational network testing with an example 6M
   b) Explain about simulation with an example 6M

UNIT–V

9. a) What is one-phase and two-phase clocking systems? Compare them 6M
   b) Explain about design validation and testing 6M

OR

10. a) Explain system-on-chip concept using platform based design 6M
    b) Explain about off–chip Connections 6M

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