Hall Ticket Number :										

R14

Code: 4PB312

M.Tech. I Semester Regular & Supplementary Examinations Feb/Mar 2016

Micro Controllers & Interfacing

(Embedded Systems)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT-I

1. a) With a neat architectural diagram, explain about 8051. 8M

   b) Explain about interrupts of 8051. 4M

OR

2. a) Discuss briefly about instructions of 8051. 8M

   b) Discuss about timer modules of 8051. 4M

UNIT-II

3. With a neat diagram, explain about 8279 keyboard and display controller. 12M

OR

4. With an example, explain about flash memory interfacing with 8051 microcontroller. 12M

UNIT-III

5. Explain about addressing modes of Motorola 68HC11 with examples. 12M

OR

6. Explain about serial communication interface and A/D conversion features of Motorola 68HC11. 12M

UNIT-IV

7. a) Discuss about register file structure of PIC 16C74. 6M

   b) Explain about program memory considerations of PIC 16C74. 6M

OR

8. a) Discuss about I/O ports of PIC 16C74. 6M

   b) Explain about UART of PIC 16C74. 6M

UNIT-V

9. With a neat diagram, explain about ARM controller architecture. 12M

OR

10. Discuss about Thumb instructions of ARM processor with examples. 12M

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Hall Ticket Number :										

R14

Code: 4PC311

M.Tech. I Semester Regular & Supplementary Examinations Feb/Mar 2016

VLSI Technology

(*Common to Embedded Systems & VLSISD*)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT-I

1. a) Derive the I_{DS} versus V_{DS} expression of a NMOS transistor. 6M
   b) Draw the simple BICMOS inverter and explain its operation. Mention its drawbacks and give suitable remedies. 6M

OR

2. a) Explain the design of CMOS inverters with neat expressions. 6M
   b) Explain the parameters G_m, G_{DS}, W_O with respect to a MOS device. 6M

UNIT-II

3. a) Explain the concept of wires. 3M
   b) Explain the scalable design rules in detail with neat diagrams. 9M

OR

4. a) Discuss the transistor structures in detail. 6M
   b) Explain the concept of layout design tools. 6M

UNIT-III

5. a) Explain the advantages and drawbacks of Static complementary gates. 6M
   b) Explain the concept of resistive interconnect delays. 6M

OR

6. a) Discuss the alternate gate circuits with neat diagrams. 6M
   b) Design a 3 input NOR gate and explain its operation. 6M

UNIT-IV

7. a) Explain the concept of Interconnect design. 6M
   b) Discuss the switch logic networks in detail. 6M

OR

8. a) Write a short note on simulation. 6M
   b) Draw the layout of a 3 input NAND gate. 6M

UNIT-V

9. a) Discuss the concept of Off chip connections. 6M
   b) Give the concept of Power optimization. 6M

OR

10. a) Explain the concept of High level synthesis in detail. 6M
    b) Discuss the concept of Clocking disciplines. 6M

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Hall Ticket Number :										

R14

Code: 4PB313

M.Tech. I Semester Regular & Supplementary Examinations Feb/Mar 2016

Real Time Operating Systems

(*Embedded Systems*)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT-I

1. a) With an example explain the following system calls for file I/O:
   (i) open
   (ii) create
   (iii) write
   b) Write a brief note on Shared Memory.

OR

2. a) With an example explain the following Process control functions:
   (i) vfork
   (ii) exit
   (iii) wait
   b) Write a brief note on Semaphores.

UNIT-II

3. Explain in detail about Periodic task model.

OR

4. a) Write a brief note on Preemptivity of resources.
   b) Describe the uses of precedence graph and task graph.

UNIT-III

5. a) Compare dynamic vs. static systems.
   b) With an example explain Round Robin approach to real time scheduling.

OR

6. a) With an example explain effective release times and deadlines.
   b) Define dynamic system.

UNIT-IV

7. a) With a neat sketch explain the hardware and software interrupt priorities.
   b) Discuss in brief about asynchronous timer functions.

OR

8. Explain the following:
   (a) Preemption lock
   (b) Release guard mechanism

UNIT-V

9. a) Discuss the different types of faults
   b) Explain in brief about Core RT Linux.

OR

10. a) Briefly explain about integrated failure handling.
    b) With an example explain the following:
    (i) Pipeline
    (ii) Grouping commands

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Hall Ticket Number :										

R14

Code: 4PC313

M.Tech. I Semester Regular & Supplementary Examinations Feb/Mar 2016

Digital IC Design

(Common to Embedded Systems & VLSI System Design)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT-I

1. Design Static CMOS inverter and analyze its behavior using switch models. 12M

OR

2. a) Describe significant advantages of dynamic logic over static logic. 6M

   b) What are all the effects of supply voltage scaling in CMOS inverter? Explain in brief. 6M

UNIT-II

3. a) What are the advantages of NORA logic? Also explain the need of NORA logic. 6M

   b) Design a full adder using Domino logic gates. 6M

OR

4. Design 3 to 8 decoder in NORA logic. Use 2 to 4 decoder while implementing 3 to 8 decoder. 12M

UNIT-III

5. a) Explain the adiabatic approach to CMOS VLSI design technique. 6M

   b) Derive the expression for short circuit power consumption in CMOS circuits and relate drain current (I_D), drain voltage (V_{DD}). 6M

OR

6. a) Define guard evolution. Explain its role in switching activity of CMOS XOR logic circuit. 6M

   b) Explain how bus multiplexing effects on logic effort in CMOS NAND gate. Find its logic effort value. 6M

UNIT-IV

7. a) What are the precautions to be taken during global routing and mention its layout lambda based design limitations for CMOS. 6M

   b) Calculate the equivalent sheet resistance for two NMOS inverters connected in cascaded. Assume $\left(\frac{W}{L}\right)_p = 60$, $\left(\frac{W}{L}\right)_n = 40$, Sheet resistance as R_s, Delay time as T. 6M

OR

8. a) Explain the function to drive large capacitance load (C_{LOAD}) in low power CMOS circuits. Find the resonance frequency f_{RES} in terms of R_{LOAD} and C_{LOAD}. 6M

   b) Describe full custom layout design for CMOS circuit. 6M

UNIT-V

9. a) Write the design procedure for Modified Booth Multiplier. 6M

   b) Give the transistor level realization of Adder/ Subtractor. 6M

OR

10. a) What are the design criteria reviewed in CMOS static RAM cell design? 6M

    b) Explain how ALU functions implemented using adders and multipliers. 6M

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Hall Ticket Number :										

R14

Code: 4PC315

M.Tech. I Semester Regular & Supplementary Examinations Feb/Mar 2016

FPGA Architectures and Applicaitons

(*Common to Embedded Systems & VLSISD*)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT-I

1. a) Distinguish between Altera's MAX 5000 and MAX7000 series PLDS. 6M
   b) Explain Cypres Flash 370 Device Technology. 6M

OR

2. a) With a neat sketch of MAX 5000 device macro cell. Explain how the sequential logic is implemented. 6M
   b) Implement the following Boolean function using a suitable PAL
   F(a, b, c, d) = Σm(2,4,6,8,10,11,12,14,15). 6M

UNIT-II

3. a) Draw and explain logic blocks of FPGAs. 6M
   b) List the Actel based FPGAs and give their speed performance. 6M

OR

4. a) Distinguish between FPGA Design Flow and ASIC Design Flow. Explain FPGA Routing Architecture with all the steps. 6M
   b) Explain the Technology mapping for FPGAs. 6M

UNIT-III

5. a) Give brief comparison of Act1, Act2 and Act3 FPGAS. 6M
   b) What are the salient features of Altera's FLEX 8000 FPGA logic element? 6M

OR

6. a) Explain the AT & T-ORACs (Optimized Reconfigurable Cell Array). 6M
   b) Speed performance in system programmability. 6M

UNIT-IV

7. Draw a state diagram for a sequence checker, whose output will be '1' whenever the sequence 1011 is detected. Develop a one-hot design for the same sequence checker. 12M

OR

8. a) What are the features of the extended Petri Nets used for parallel controllers? 6M
   b) Explain the Micro-programing linked state machine with an example. 6M

UNIT-V

9. a) Explain FSM architectures centered around non-registered PLDs. 6M
   b) With suitable example, explain system level design by considering controller, data path. 6M

OR

10. a) Explain the design approach of state machines centered around shift registers. 6M
    b) With an example explain about One-Hot design method using ASMs. 6M

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Hall Ticket Number :										

R14

Code: 4PB311

M.Tech. I Semester Regular & Supplementary Examinations Feb/Mar 2016

Embedded System Concepts

(Common to DECS, Embedded Systems, VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT-I

1. Discuss the following in details
   i) Characteristics and constraints of embedded systems
   ii) Classifications of embedded systems 12M

OR

2. Explain about significance of each hardware unit present in embedded design 12M

UNIT-II

3. a) Compare Harvard and Princeton memory organizations. 4M
   b) Why should a program be divided into functions (routines or modules) and each placed in different memory blocks or segments 8M

OR

4. What are the different memories, input and output devices used In embedded systems? How will you interface these input and output devices in embedded systems 12M

UNIT-III

5. What is meant by scheduling? How do schedule the tasks with different algorithms 12M

OR

6. Explain about different buses used in parallel communication between networked devices 12M

UNIT-IV

7. What is meant by co-design? Explain design & co-design issues in system development process 12M

OR

8. Discuss different design methodologies for embedded system. 12M

UNIT-V

9. Describe the classes, the objects which are used in writing codes for saving an image file in a digital camera? 12M

OR

10. How do you design an automatic chocolate vending machine? Explain clearly. 12M

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