Hall Ticket Number :										

R14

Code: 4PB321

M.Tech. II Semester Regular & Supplementary Examinations Aug/Sep 2016

Testing & Testability

(Common to E.Sys & VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. a) With a neat diagram, explain about gate level event driven simulation with an example. 08M

   b) Discuss about structural models. 04M

OR

2. a) What is logic simulation? Discuss about types of simulation with examples. 08M

   b) Discuss about different levels of modeling digital circuits. 04M

UNIT-II

3. a) Describe various fault models for combinational circuits with examples. 08M

   b) Give a few fault simulation applications. 04M

OR

4. Discuss about the following stages of fault diagnosis.
   (a) Fault detection (b) Fault Equivalence (c) Fault Location 12M

UNIT-III

5. With necessary diagrams, describe the functional testing of a sequential circuit with a specific fault model. 12M

OR

6. With an example and necessary diagram discuss about signature analysis. 12M

UNIT-IV

7. Discuss about board level and system level DFT applications with examples. 12M

OR

8. a) Discuss about boundary scan standards 06M

   b) Explain with examples (i) Controllability and (ii) Absorbability 06M

UNIT-V

9. Discuss about the following testing features with examples,
   (a) ICT (b) JTAG 12M

OR

10. Discuss about the following BIST architectures:
    (a) CBIST (b) BILBO (c) CATS (d) CSTP 12M

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Hall Ticket Number :										

R14

Code: 4PB322

M.Tech. II Semester Regular & Supplementary Examinations Aug/Sep 2016

Embedded software Design

(Embedded Systems)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. a) With a neat sketch explain Pentium microprocessor organization? 6M
   b) Discuss functions of special registers in a Pentium processor. 6M

OR

2. a) Explain special features of super scalar architecture pertaining to Pentium processor 6M
   b) Describe memory management unit in a Pentium processor 6M

UNIT-II

3. Explain selection process in an embedded system design. 12M

OR

4. Explain in detail about embedded design life cycle with an example. 12M

UNIT-III

5. Write note on Basic tool set used in embedded system software design. 12M

OR

6. Explain how interrupt mechanism works in embedded system. What is its significance? Discuss with one example 12M

UNIT-IV

7. Discuss different functional tests used to test embedded software? 12M

OR

8. a) Explain terms Real time track and Hardware Break points. 6M
   b) Explain the advantages and disadvantages of back ground debug mode. 6M

UNIT-V

9. a) Discuss various kinds of buffers & explain the reasons for occurring over and under–run states 6M
   b) Write note on Native compilers versus Cross- Compliers. 6M

OR

10. Write note on
    a) Buffer Exchange 4M
    b) Porting Kernels 4M
    c) Memory and performance Trade-offs 4M

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Hall Ticket Number :										

R14

Code: 4PB323

M.Tech. II Semester Regular & Supplementary Examinations Aug/Sep 2016

Hardware Software Co-Design

(Common to Embedded Systems & VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. a) Describe the issues of co-design which are required for hardware architectures in embedded systems. 6M

   b) With a flow diagram explain the principle of generic co-design methodology 6M

OR

2. a) How hardware software partitioning algorithms for co-synthesis applications play an important role in embedded system design? 6M

   b) Explain briefly, Co-synthesis algorithm which is used for different Models of Software Partitioning 6M

UNIT-II

3. a) How prototyping and emulation can reach the goal of 'First-Time-Right-Silicon' in hardware software co-design? 6M

   b) What are the non-functional constraints which influence on design objectives and architectures of embedded systems? 6M

OR

4. Compare Architectures for control dominated systems with data dominated systems in classifying Target architectures for embedded systems 12M

UNIT-III

5. Discuss the design tools of embedded software development needs of embedded processors and ASIPs 12M

OR

6. a) List out the design tools of embedded software development needs of embedded processors and its importance. 6M

   b) Discuss about the Mixed systems and Less specialized systems with Applications 6M

UNIT-IV

7. Bring out the number of alternative ways of coordinating concurrent computations in co-designed system. 12M

OR

8. Describe the kinds of formal verification methods used at different stages of the design process. 12M

UNIT-V

9. Why different techniques are introduced for heterogeneous specifications and multi-language co-simulation? Discuss. 12M

OR

10 a) Write a short notes on the system level synthesis and its Design 6M

   b) Discuss briefly on the co-design computational model 6M

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Hall Ticket Number :										

R14

Code: 4PB325

M.Tech. II Semester Regular & Supplementary Examinations Aug/Sep 2016

Modelling and Synthesis through Verilog HDL

(Embedded Systems)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. a) Why do we need HDLs? What do we need from HDLs? 4M

   b) Write Verilog code for Half adder with neat block diagram and truth tables. Write test bench Verilog code for Half adder 8M

OR

2. Explain about various Operators available in Verilog with suitable examples. 12M

UNIT-II

3. Write Verilog programme for AOI logic circuit with suitable circuit diagram in Behavioral modeling? Write the test bench porgramme for AOI logic circuit 12M

OR

4. Write about Delays in Verilog with suitable examples? 12M

UNIT-III

5. Draw and Write code for switch level design of 2-input NAND, 2-input NOR and Inverter in Verilog? Explain its operation. 12M

OR

6. Explain Blocking and non-blocking assignments in Verilog with suitable examples? 12M

UNIT-IV

7. What is synthesis of Combinational circuits? Explain. 12M

OR

8. What is FSM of Sequence detector in Verilog? Explain 12M

UNIT-V

9. Synthesis of fork - join blocks and disable statements? Explain 12M

OR

10. Explain about synthesis of various Loops for language constructs 12M

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Hall Ticket Number :										

R14

Code: 4PB326

M.Tech. II Semester Regular & Supplementary Examinations Aug/Sep 2016

Radio Frequency Identification

(Embedded Systems)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. a) State components of an RFID system and briefly explain. 6M

   b) Explain the transponder construction format of Tool and Gas Bottle identification keys. 6M

OR

2. Illustrate the selection criteria for RFID system with respect to Operating frequency range. 12M

UNIT-II

3. Describe Surface Acoustic wave Transponder 12M

OR

4. Explain the measurement of transponder resonant frequency and Coupling coefficient in RFID systems. 12M

UNIT-III

5. a) Explain the procedure for measuring the physical variables using Microwave transponder 6M

   b) Briefly explain Security Logic memory. 6M

OR

6. Explain FSK and PSK modulation procedures. 12M

UNIT-IV

7. Describe CRC and ALOHA procedures. 12M

OR

8. Describe Anti-collision procedures with one example and attacks on RFID systems. 12M

UNIT-V

9. Explain Visa Contactless and public transport. 12M

OR

10. Explain briefly about NFC applications and electronic Passport Transport systems. 12M

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Hall Ticket Number :										

R14

Code: 4PB324

M.Tech. II Semester Regular & Supplementary Examinations Aug/Sep 2016

DSP Processors and Architectures

(Common to DECS Embedded Systems & VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. a) Perform an implementation for an 8-point DIT FFT algorithm which includes spectrum computation using FFT result 8M

   b) Explain Dynamic Range and precision in Detail 4M

OR

2. Differentiate A/D Conversion errors and D/A Conversion errors relevant to computational accuracy in DSP applications. 12M

UNIT-II

3. Explain the features for external interfacing in connection with programmable DSP devices. 12M

OR

4. a) With suitable example explain the data addressing capabilities for programmable DSP devices. 8M

   b) What is Braun multiplier? Explain 4X4 Braun multiplier 4M

UNIT-III

5. a) Explain the data addressing model of TMS320C45XX processors in detail. 8M

   b) WAP to implement PID controller on TMS320C54XX processor. 4M

OR

6. What are different interrupts of TMS320C54XX processor? Explain them. 12M

UNIT-IV

7. a) Explain about Adaptive filters in detail. 4M

   b) Discuss about Bit- reversed generation in detail. 8M

OR

8. Describe the sources of error for evaluating the computational accuracy in DSP implementations. 12M

UNIT-V

9. With suitable diagram explain the concept of memory interfacing to programmable DSP devices 12M

OR

10. a) Explain the memory space organization of programmable DSP devices with simple example 8M

    b) Explain a CODEC Interface circuit with its necessary programming by considering an example. 4M

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