Hall Ticket Number :										

R14

Code: 4PB321

M.Tech. II Semester Regular & Supplementary Examinations Aug/Sep 2016

Testing & Testability

(Common to E.Sys & VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. a) With a neat diagram, explain about gate level event driven simulation with an example. 08M

   b) Discuss about structural models. 04M

OR

2. a) What is logic simulation? Discuss about types of simulation with examples. 08M

   b) Discuss about different levels of modeling digital circuits. 04M

UNIT-II

3. a) Describe various fault models for combinational circuits with examples. 08M

   b) Give a few fault simulation applications. 04M

OR

4. Discuss about the following stages of fault diagnosis.
   (a) Fault detection (b) Fault Equivalence (c) Fault Location 12M

UNIT-III

5. With necessary diagrams, describe the functional testing of a sequential circuit with a specific fault model. 12M

OR

6. With an example and necessary diagram discuss about signature analysis. 12M

UNIT-IV

7. Discuss about board level and system level DFT applications with examples. 12M

OR

8. a) Discuss about boundary scan standards 06M

   b) Explain with examples (i) Controllability and (ii) Absorbability 06M

UNIT-V

9. Discuss about the following testing features with examples,
   (a) ICT (b) JTAG 12M

OR

10. Discuss about the following BIST architectures:
    (a) CBIST (b) BILBO (c) CATS (d) CSTP 12M

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Hall Ticket Number :										

R14

Code: 4PC321

M.Tech. II Semester Regular & Supplementary Examinations Aug/Sep 2016

Low Power VLSI Design

(VLSI System Design)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. a) Draw and explain high performance, high cost digital Bi-CMOS process using Twin-well process. 6M
   b) Explain the punch through (Surface DIBL) in short channel MOSFETs. 6M

OR

2. a) Explain the Deep Trench Isolation technique in Bi-CMOS process. 6M
   b) Explain the considerations for process integration in integrated analog/digital Bi-CMOS process. 6M

UNIT-II

3. Explain the trends and directions of CMOS/ Bi-CMOS deep submicron process. 12M

OR

4. a) Explain SOI CMOS/ Bi-CMOS VLSI deep submicron process in detail. 6M
   b) Explain low-voltage/low-power lateral BJT on SOI process. 6M

UNIT-III

5. a) Explain BSIM3 version 3 threshold voltage and current models. 6M
   b) Discuss the salient features of EKV MOSFET model. 6M

OR

6. a) Draw and discuss the Ebers-Moll bipolar spice model. 6M
   b) Discuss the static and dynamic characteristics of a MOSFET with neat sketches. 6M

UNIT-IV

7. Compare and contrast the three Bi-CMOS basic driver configurations with neat sketches. 12M

OR

8. a) Explain ESD-free Bi-CMOS digital circuit with a neat diagram and mention its advantages. 6M
   b) Draw a three input CMOS NAND gate and explain its operation. 6M

UNIT-V

9. a) Explain the design perspective of single edge-triggered flip-flops. 6M
   b) Explain the design perspective of double edge-triggered flip-flops. 6M

OR

10. a) Explain low power techniques for SRAM in brief. 6M
    b) Explain Power reduction techniques in clock networks in brief. 6M

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Hall Ticket Number :										

R14

Code: 4PB323

M.Tech. II Semester Regular & Supplementary Examinations Aug/Sep 2016

Hardware Software Co-Design

(Common to Embedded Systems & VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. a) Describe the issues of co-design which are required for hardware architectures in embedded systems. 6M

   b) With a flow diagram explain the principle of generic co-design methodology 6M

OR

2. a) How hardware software partitioning algorithms for co-synthesis applications play an important role in embedded system design? 6M

   b) Explain briefly, Co-synthesis algorithm which is used for different Models of Software Partitioning 6M

UNIT-II

3. a) How prototyping and emulation can reach the goal of 'First-Time-Right-Silicon' in hardware software co-design? 6M

   b) What are the non-functional constraints which influence on design objectives and architectures of embedded systems? 6M

OR

4. Compare Architectures for control dominated systems with data dominated systems in classifying Target architectures for embedded systems 12M

UNIT-III

5. Discuss the design tools of embedded software development needs of embedded processors and ASIPs 12M

OR

6. a) List out the design tools of embedded software development needs of embedded processors and its importance. 6M

   b) Discuss about the Mixed systems and Less specialized systems with Applications 6M

UNIT-IV

7. Bring out the number of alternative ways of coordinating concurrent computations in co-designed system. 12M

OR

8. Describe the kinds of formal verification methods used at different stages of the design process. 12M

UNIT-V

9. Why different techniques are introduced for heterogeneous specifications and multi-language co-simulation? Discuss. 12M

OR

10 a) Write a short notes on the system level synthesis and its Design 6M

   b) Discuss briefly on the co-design computational model 6M

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Hall Ticket Number :										

R14

Code: 4PC322

M.Tech. II Semester Regular & Supplementary Examinations Aug/Sep 2016

ASIC Design

(VLSI System Design)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. With the help of neat sketches explain about different types of MGA 12M

OR

2. a) List out the differences between the mixed mode and analogue ASICs 4M
   b) Discuss about cell based IC 8M

UNIT-II

3. Explain the different structures of PAL based PLDs 12M

OR

4. a) Describe the architecture of Xilinx xc2000 CLB 6M
   b) Describe the ACT2 and ACT3 module architecture 6M

UNIT-III

5. Explain the characteristics and performance of standard cell and cell based-ASICs with an example 12M

OR

6. Explain the characteristics and performance of Gate array ASICs with an example 12M

UNIT-IV

7. a) With an example show how the D-Calcus algorithm is used for tracing faults 8M
   b) Explain the different algorithms for fault simulation 4M

OR

8. a) How ATPG algorithm is used to generate vectors automatically 6M
   b) Explain how the problem of reconvergent fan-out is solved 6M

UNIT-V

9. a) Explain the Kernighan-Lin algorithm with an example 8M
   b) What are the goals and objectives of floor planning 4M

OR

10. a) Describe how the I/O and power constraints in ASICs are considered during floor planning 8M
    b) How the ratio-cut algorithm removes the restriction of constant partition sizes 4M

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Hall Ticket Number :										

R14

Code: 4PC323

M.Tech. II Semester Regular & Supplementary Examinations Aug/Sep 2016

Algorithms for VLSI Design Automation

(VLSI System Design)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. a) Discuss about algorithmic graph theory in brief. 6M
   b) Explain integer linear programming. 6M

OR

2. a) Discuss about design methodologies for VLSI design. 6M
   b) Explain Tabu search in detail. 6M

UNIT-II

3. a) Compare & contrast signal modeling, gate modeling and delay modeling. 6M
   b) Explain connectivity and signal modeling in brief. 6M

OR

4. a) Explain simulation mechanisms. 6M
   b) Explain Event-driven simulation. 6M

UNIT-III

5. a) Explain ROBDD implementation & construction. 6M
   b) Explain variable ordering in detail. 6M

OR

6. a) Explain two-level logic synthesis in brief. 6M
   b) Discuss about applications to verification. 6M

UNIT-IV

7. a) Write a short note on hardware for computations, data storage & interconnection. 6M
   b) Discuss the goals of allocation, assignment & scheduling. 6M

OR

8. a) Explain ASAP scheduling in brief. 6M
   b) Discuss about the optimization issues of the assignment problem in high-level synthesis. 6M

UNIT-V

9. a) Discuss about MCM physical design cycle. 6M
   b) Explain Topologic routing in brief. 6M

OR

10. a) Explain Placement-chip array based and full custom approaches. 6M
    b) Discuss about multiple stage Routing. 6M

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Hall Ticket Number :										

R14

Code: 4PB324

M.Tech. II Semester Regular & Supplementary Examinations Aug/Sep 2016

DSP Processors and Architectures

(Common to DECS Embedded Systems & VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. a) Perform an implementation for an 8-point DIT FFT algorithm which includes spectrum computation using FFT result 8M

   b) Explain Dynamic Range and precision in Detail 4M

OR

2. Differentiate A/D Conversion errors and D/A Conversion errors relevant to computational accuracy in DSP applications. 12M

UNIT-II

3. Explain the features for external interfacing in connection with programmable DSP devices. 12M

OR

4. a) With suitable example explain the data addressing capabilities for programmable DSP devices. 8M

   b) What is Braun multiplier? Explain 4X4 Braun multiplier 4M

UNIT-III

5. a) Explain the data addressing model of TMS320C45XX processors in detail. 8M

   b) WAP to implement PID controller on TMS320C54XX processor. 4M

OR

6. What are different interrupts of TMS320C54XX processor? Explain them. 12M

UNIT-IV

7. a) Explain about Adaptive filters in detail. 4M

   b) Discuss about Bit- reversed generation in detail. 8M

OR

8. Describe the sources of error for evaluating the computational accuracy in DSP implementations. 12M

UNIT-V

9. With suitable diagram explain the concept of memory interfacing to programmable DSP devices 12M

OR

10. a) Explain the memory space organization of programmable DSP devices with simple example 8M

    b) Explain a CODEC Interface circuit with its necessary programming by considering an example. 4M

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