Code: 4PA321

R-14

M. Tech. II-Semester Regular Examinations Oct/Nov 2015

Coding Theory and Techniques

(DECS)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. a) Prove that I(X,Y)=H(X)-H(X/Y) 6M

   b) A Transmitter has an alphabet of four letters [x_1, x_2, x_3, x_4] and the receiver has an alphabet of Three letters[y_1, y_2, y_3].The joint Probability matrix is

$$P(X,Y)=\begin{bmatrix} 0.3 & 0.05 & 0 \\ 0 & 0.25 & 0 \\ 0 & 0.15 & 0.05 \\ 0 & 0.05 & 0.15 \end{bmatrix}$$

   . Calculate H(X), H(Y), H(X/Y) and H(Y/X) 6M

OR

2. a) Explain the following

   i) Mutual Information

   ii) Entropy 6M

   b) Construct the Huffman code for the following symbols with associated probabilities and calculate the coding efficiency

Symbol	A	B	C	D	E	F	G
probability	0.2	0.16	0.14	0.08	0.22	0.07	0.13

6M

UNIT-II

3. The parity check bits of (8,4) block code are generated by

   $C_5=d_1+d_2+d_4$, $C_6=d_1+d_2+d_3$, $C_7=d_1+d_4+d_3$, $C_8=d_4+d_2+d_3$ where d_1, d_2, d_3 ,d_4 are the message digits.

   i) Find the generator matrix and parity check matrix for this code

   ii) Find the minimum weight of this code

   iii) Find the error detection capability of this code 12M

OR

4. a) Explain the about the Reed-Muller codes by generator matrix with example 8M

   b) Explain the properties of Reed-Muller codes by generator matrix 4M

UNIT-III

5. a) A (15,5) linear cyclic code has a generator polynomial

   $g(x)=1+x+x^2+x^4+x^5+x^8+x^{10}$

   (a) Find the code polynomial for the message polynomial $D(x)= 1+x^2+x^4$[in systematic form]

   (b) Is $V(x)= 1+x^4+x^6+x^8+x^{10}+x^{14}$ a code polynomial ?If not find the syndrome 8M

   b) Explain the Binary Cyclic code properties 4M

OR

6. a) Explain the process of systematic and non-systematic form of encoding 6M

   b) Explain the Encoder using (n-k) bit shift register with neat sketch 6M

UNIT-IV

7. Draw the state diagram, tree diagram and trellis's diagram for k=3, rate1/3 code generated by $g_1(x)=1+x^2$, $g_2(x)=1+x$ and $g_3(x)=1+x+x^2$ 12M

OR

8. Explain about the following
   a) Fano Sequential Decoding Algorithm
   b) Majority Logic Decoding 12M

UNIT-V

9. a) Write a short note on Galois fields 6M
   b) List out and elaborate the basic properties of Galois Fields 6M

OR

10. a) Write short note on BCH Codes 6M
    b) Explain the Decoding procedure for BCH codes 6M

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M.J. Damodhar

Code: 4PA322

R-14

M. Tech. II-Semester Regular Examinations Oct/Nov 2015

High Speed Networks

(DECS)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. a) Differentiate the different types of services provided by Networks to its users. 6M
   b) With the help of diagram, write about Virtual circuit switching. Also explain how it is a compromise between circuit switching and packet switching. 6M

OR

2. a) Write about the benefits offered by ISDN and B-ISDN. 6M
   b) Discuss the evolution of B-ISDN and explain the functional architecture of B-ISDN. 6M

UNIT-II

3. a) Write about virtual channels and virtual paths in ATM networks. 6M
   b) Draw the structure of ATM cell header and explain about all the fields in detail. 6M

OR

4. Draw and explain about ATM Layered architecture. 12M

UNIT-III

5. a) Mention features of Re-arrangeable networks 6M
   b) What is blocking in Banyan Networks? Explain how blocking can be avoided in Batcher- Banyan Network. 6M

OR

6. a) Distinguish between Banyan and Benes networks 6M
   b) Explain the operation of a cross bar switch. Design a (4, 4, 4) symmetric three stage clos network. 6M

UNIT-IV

7. a) Distinguish between UNI and PNNI signaling. 6M
   b) Explain about ABR Traffic management. 6M

OR

8. Explain PNNI routing mechanism with a suitable example. 12M

UNIT-V

9. a) Draw and explain about IPV4 header format. 6M
   b) Address the differences between IPV4 and IPV6 protocols. 6M

OR

10. a) With the help of dynamics of congestion window, explain about TCP congestion control algorithm 6M
    b) Write short notes on differentiated and integrated services 6M

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Code: 4PA323 **R-14**

M. Tech. II-Semester Regular Examinations Oct/Nov 2015

Micro Computer System Design

(DECS)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. a) Bring out the architectural and signal difference between the 8086 and 8088? 6M
   b) Give the difference and flag settings for SF, ZF, CF, OF and PF after subtracting 4AE0 from each of the following?
   (i) 1234 (ii) 5D90 6M

OR

2. a) Draw the register organization of 8086 and explain typical applications of each register? 6M
   b) Explain the arithmetic and logical instructions of 8086 with examples. 6M

UNIT-II

3. a) What are the differences between logical address, linear address and physical address? 6M
   b) Enlist the data types supported by 80486? 6M

OR

4. How many maximum descriptors can be accessed by 80386 for single task? What is memory addressing capability of single descriptor? Justify the virtual memory addressing capability of 80386 per task? 12M

UNIT-III

5. a) Explain about 64-bit extension technology of Pentium 4 and core 2 processors 8M
   b) Thread Level Parallelism (TLP). 4M

OR

6. Write short notes on :
   i). Trace cache
   ii).SSE instructions
   iii).Out of order execution 12M

UNIT-IV

7. a) What is mean by common procedure sharing? Explain the reentrant code shared by more than one processor? 6M
   b) What is mean by semaphore? Explain it operations with an example? 6M

OR

8. What are the different states present in simple multiprogramming system? Explain each of them with the help of state diagram? 12M

UNIT-V

9. a) Write and explain the Data formats for the SSE 2 and SSE 3 instructions. 6M
   b) Draw and explain Memory format for the FSTENV instructions. 6M

OR

10. a) Explain about the MMX Technology 6M
    b) Draw and explain the 80X87 arithmetic coprocessor status register. 6M

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Hall Ticket Number :

R-14

Code: 4PA324

M. Tech. II-Semester Regular Examinations Oct/Nov 2015

Detection and Estimation of Signals

(DECS)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. a) State and prove the following properties of Discrete Fourier Transform. i)Multiplication in time domain ii) differentiation in frequency domain 6M

   b) Find and sketch the Fourier Transform of the discrete time impulse train x(n) = $\sum_{m=-\infty}^{\infty}\delta(n-mN)$ 6M

OR

2. a) Establish the relationship between input and output Energy Spectral Densities of an LTI System 6M

   b) Determine and sketch the magnitude and phase response of the system y(n)= $\frac{1}{2}[x(n+1)+x(n-1)]$ 6M

UNIT-II

3. Explain the mathematical detection problem for detection of signals in the presence of noise. 12M

OR

4. Explain the minimum probability of error and Bayes risk criterion for the detection of signals. 12M

UNIT-III

5. a) Derive the expression for the impulse response of a matched filter 6M

   b) Consider a signal s(t)= A cos(2*pi*f_c*t) for 0≤t≤T given as a input to a matched filter determine the impulse response and hence the output of the matched filter. What happens to the output when t=T? 6M

OR

6. Explain about different linear models for the deterministic signals. 12M

UNIT-IV

7. Explain the Maximum Likelihood ratio test for the detection of signals in noise. 12M

OR

8. Explain the composite hypothesis testing for the detection of signals in the presence of noise. 12M

UNIT-V

9. a) Explain the maximum likelihood estimates of the parameters of linear system. 6M

   b) Explain the following i) MAP estimate ii) posteriori density function 6M

OR

10. Explain the least mean squares algorithm for the estimation of signals. 12M

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Hall Ticket Number :

R-14

Code: 4PA325

M. Tech. II-Semester Regular Examinations Oct/Nov 2015

Image and Video Processing

(DECS)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. a) An Image is given by $f(x,y)=\begin{bmatrix}1&1&2&1\\2&1&1&2\\1&3&2&1\\2&1&2&1\end{bmatrix}$ find the 2D Hadamard Transform for this Image matrix 6M

   b) Explain the following properties of DFT i)Correlation ii) Scaling 6M

OR

2. a) Find the Eigen value and Eigen vector of the following matrix $A=\begin{bmatrix}4&1\\3&2\end{bmatrix}$ 6M

   b) Show how the KL Transform is useful for reducing the dimensions of an Image 6M

UNIT-II

3. a) What would be the Impact of removing the LSB of the pixel values in the histogram of the following image $f(x,y)=\begin{bmatrix}6&7&1\\5&1&4\\1&2&3\end{bmatrix}$ 6M

   b) Explain about histogram equalization 6M

OR

4. a) Discuss about Image Smoothing and Sharpening filter in Spatial Domain 6M

   b) Explain the Frequency Domain Techniques for Image Enhancement 6M

UNIT-III

5. a) Explain the concept of Inverse filtering and what are the Limitations of it? 6M

   b) Distinguish between Image Enhancement and Image Restoration 6M

OR

6 a) A blur filter is given by $h(m,n)=\begin{bmatrix}1&1&1&1\\1&2&2&1\\1&2&2&1\\1&1&1&1\end{bmatrix}$ design a deblur filter h(k,l) Using Inverse filter approach 6M

   b) Using Weiner filter approach given that the Signal and Noise Variances are 200 and 50 respectively 6M

UNIT-IV

7. a) Discuss the Huffman coding with an example 6M
   b) Explain how Tredictive Coding Technique eliminate the interpixel redundancy 6M

OR

8. a) Explain the concept of Image segmentation using variable thresholding 6M
   b) A 1024X1024 8-bit image with 4.2 bits/pixel entropy is to be Huffman coded
      i) what is the maximum compression that can be expected
      ii) if a greater level of lossless compression is required, what else can be done 6M

UNIT-V

9. a) Discuss the concept of digital video transmission 6M
   b) Explain about motion estimation criteria 6M

OR

10. a) What are various digital video formats used in video representation? Explain the relevant equations, various video quality measures. 8M
    b) Explain the formation of digital video. 4M

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Hall Ticket Number :

Code: 4PB324

R-14

M. Tech. II-Semester Regular Examinations Oct/Nov 2015

DSP Processors and Architectures

(Common to DECS, Embedded Systems & VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. Explain FFT algorithm for DFT computation with the help of butterfly diagram in detail 12M

OR

2. a) What are the various types of discrete time sequences in DSP for analysis purpose and give their definitions and MATLAB representations 8M

   b) Write Short notes on Compensating filter. 4M

UNIT-II

3. a) Explain Bus architecture & speed issues of programmable DSP devices. 8M

   b) Explain the basic architectural features considered for programmable DSP devices. 4M

OR

4. Describe the sources of error for evaluating the computational accuracy in DSP implementations. 12M

UNIT-III

5. Write a program to implement decimation & interpolation on TMS320C54XX 12M

OR

6. a) Explain the six-levels of pipeline structure of TMS320C54XX processor. 8M

   b) What is Q-notation? How it is used for DSP implementations? 4M

UNIT-IV

7. a) What is the role of anti aliasing and reconstruction filters in DSP system? 8M

   b) Write short notes on FIR and IIR filter in all respects. 4M

OR

8. Explain the features for external interfacing in connection with programmable DSP devices. 12M

UNIT-V

9. a) Explain how to interface the parallel I/O peripherals to programmable DSP devices with suitable example 8M

   b) Explain MCBSP in detail. 4M

OR

10. a) Write about CODEC interfacing circuit with neat sketch. 8M

    b) What are different external bus interfacing signals? In detail. 4M

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