Code: 4PB321

R-14

M. Tech. II-Semester Regular Examinations Oct/Nov 2015

Testing & Testability

(Common to E.Sys & VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. a) With examples, describe the concepts of modeling digital circuits at gate level and register level. 08M

   b) Discuss about hazard detection. 04M

OR

2. a) With examples and with relevant diagrams discuss about types of simulation 08M

   b) Discuss about any two delay models. 04M

UNIT-II

3. Describe with examples, the single stuck and multiple stuck fault models for combinational circuits. 12M

OR

4. a) Describe the fault simulation models with examples. 06M

   b) What are redundant faults? Explain with examples 06M

UNIT-III

5. a) Explain about ATPG for SSFs in sequential circuits. 06M

   b) Explain how ATPG tool is selected with an example. 06M

OR

6. a) Discuss about various compression techniques with examples. 06M

   b) Describe the concept of syndrome testing with an example. 06M

UNIT-IV

7. With the help of a neat block diagram, explain about the scan architecture and testing with an example. 12M

OR

8. Describe how the generic boundary scan is performed with relevant examples. 12M

UNIT-V

9. Discuss about the following BIST architectures: 12M

   (a) CSBL (b) BEST (c) LOCST (d) STUMPS

OR

10. With an example, describe the design procedure for self test at board level 12M

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Mr. M. Sreenath

Code: 4PB322

R-14

M. Tech. II-Semester Regular Examinations Oct/Nov 2015

Embedded Software Design

(Embedded Systems)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. a) Explain special features available in Pentium microprocessor compared to 80486 6M
   b Explain the functioning of memory management unit in a Pentium processor 6M

OR

2. a) Explain super scalar architecture of Pentium processor 6M
   b) Discuss functions of special registers in a Pentium processor 6M

UNIT-II

3. Write note on hardware and software design for specific application 12M

OR

4. Explain the challenges involved in integrating hardware and software in embedded system design 12M

UNIT-III

5. a) Write note on memory organization and its significance in embedded system design? 6M
   b) Write note on Host based debugging and debug kernels 6M

OR

6. Explain Interrupt service routine and Watch dog timer. Explain how they are different in their functionalities 12M

UNIT-IV

7. a) Explain back ground debug mode. What are the advantages and disadvantages of back ground debug mode? 8M
   b) Explain bullet proof run control. 4M

OR

8. a) Explain the significance of JTAG & Nexus in embedded firmware. 6M
   b) Explain the concept of overlay memory. 6M

UNIT-V

9. a) Explain the compilation process in embedded system with block diagram. 6M
   b) Explain Library generation procedure in embedded software. 6M

OR

10. Explain terms
    a) Buffer over run 4M
    b) Memory leakage 4M
    c) Double buffering 4M

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Code: 4PB323

R-14

M. Tech. II-Semester Regular Examinations Oct/Nov 2015

Hardware Software Co-Design

(Common to Embedded Systems & VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. a) Discuss the languages which are essential used in co-design model 6M
   b) With a flow diagram explain the principle of generic co-design methodology 6M

OR

2. a) Explain briefly, Co-synthesis algorithm which is used for different Models of Software Partitioning 6M
   b) How co-synthesis methods for distributed computing systems are different from single rate design systems? 6M

UNIT-II

3. a) Explain prototyping and emulation Techniques based on hardware, software co-design with examples 6M
   b) What are the Target Architectures and explain with the help of applications 6M

OR

4. Compare Architectures for control dominated systems with data dominated systems in classifying Target architectures for embedded systems. 12M

UNIT-III

5. a) List out the design tools of embedded software development needs of embedded processors and its importance. 6M
   b) Discuss about the Mixed systems and Less specialized systems with Applications 6M

OR

6. Discuss the pragmatic issues in setting up a compiler environment for embedded systems. 12M

UNIT-IV

7. a) Explain briefly, Coordinating concurrent computations classifications 6M
   b) List out the Verification tools and explain its 6M

OR

8. a) Distinguish between System level specification languages with examples 6M
   b) Discuss about System level specification languages with applications 6M

UNIT-V

9. a) Write a short notes on the system level synthesis and its Design 6M
   b) Discuss briefly on the co-design computational model 6M

OR

10. Why different techniques are introduced for heterogeneous specifications and multi-language co-simulation? Discuss. 12M

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Hall Ticket Number :

Code: 4PB324

R-14

M. Tech. II-Semester Regular Examinations Oct/Nov 2015

DSP Processors and Architectures

(Common to DECS, Embedded Systems & VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. Explain FFT algorithm for DFT computation with the help of butterfly diagram in detail 12M

OR

2. a) What are the various types of discrete time sequences in DSP for analysis purpose and give their definitions and MATLAB representations 8M

   b) Write Short notes on Compensating filter. 4M

UNIT-II

3. a) Explain Bus architecture & speed issues of programmable DSP devices. 8M

   b) Explain the basic architectural features considered for programmable DSP devices. 4M

OR

4. Describe the sources of error for evaluating the computational accuracy in DSP implementations. 12M

UNIT-III

5. Write a program to implement decimation & interpolation on TMS320C54XX 12M

OR

6. a) Explain the six-levels of pipeline structure of TMS320C54XX processor. 8M

   b) What is Q-notation? How it is used for DSP implementations? 4M

UNIT-IV

7. a) What is the role of anti aliasing and reconstruction filters in DSP system? 8M

   b) Write short notes on FIR and IIR filter in all respects. 4M

OR

8. Explain the features for external interfacing in connection with programmable DSP devices. 12M

UNIT-V

9. a) Explain how to interface the parallel I/O peripherals to programmable DSP devices with suitable example 8M

   b) Explain MCBSP in detail. 4M

OR

10. a) Write about CODEC interfacing circuit with neat sketch. 8M

    b) What are different external bus interfacing signals? In detail. 4M

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Hall Ticket Number :

R-14

Code: 4PB325

M. Tech. II-Semester Regular Examinations Oct/Nov 2015

Modelling and Synthesis through Verilog HDL

(Embedded Systems)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. Write about Structural (Top-down) design methodology in Verilog 12M

OR

2. How Numbers are represented in Verilog? Explain with suitable examples 12M

UNIT-II

3. Explain about User-Defined Primitives (UDP) available in Verilog. 12M

OR

4. Write about Delays in Verilog with suitable examples? 12M

UNIT-III

5. Draw and Write code for switch level design of 2-input NAND, 2-input NOR and Inverter in Verilog? Explain its operation. 12M

OR

6. Explain behavioral models of Finite State Machine (FSM). 12M

UNIT-IV

7. What is the Synthesis methodology adapted in Verilog? 12M

OR

8. What is synthesis of Latches? Explain with examples 12M

UNIT-V

9. Write about synthesis of nets, register variables and integers in Verilog? 12M

OR

10. Synthesis of Arithmetic, shift and relational operators? Explain. 12M

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Hall Ticket Number :

R-14

Code: 4PB326

M. Tech. II-Semester Regular Examinations Oct/Nov 2015

Radio Frequency Identification

(Embedded Systems)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. Explain various Transponder construction formats in RFID systems. 12M

OR

2. a) Distinguish between different RFID systems. 6M

   b) Explain the procedure of information processing in the transponder. 6M

UNIT-II

3. Explain the operation procedure involved in electromagnetic Backscatter coupling. 12M

OR

4. Explain the selection of a suitable frequency for inductively coupled RFID systems. 12M

UNIT-III

5. a) What is meant by RF Interface address and security logic memory? And briefly explain. 6M

   b) Briefly explain Dual Interface card 6M

OR

6. Describe Bipolar Phase shift keying (BPSK) modulation procedure in the transponders. 12M

UNIT-IV

7. Explain the involvement of FDMA and TDMA procedures in the Security of RFID systems. 12M

OR

8. Explain the RF interface protection by Cryptographic measures. 12M

UNIT-V

9. Explain Contactless Smart cards and Visa Contactless. 12M

OR

10. Describe various Electronic Passport Transport Systems. 12M

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