Code: 4PB321

R-14

M. Tech. II-Semester Regular Examinations Oct/Nov 2015

Testing & Testability

(Common to E.Sys & VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. a) With examples, describe the concepts of modeling digital circuits at gate level and register level. 08M

   b) Discuss about hazard detection. 04M

OR

2. a) With examples and with relevant diagrams discuss about types of simulation 08M

   b) Discuss about any two delay models. 04M

UNIT-II

3. Describe with examples, the single stuck and multiple stuck fault models for combinational circuits. 12M

OR

4. a) Describe the fault simulation models with examples. 06M

   b) What are redundant faults? Explain with examples 06M

UNIT-III

5. a) Explain about ATPG for SSFs in sequential circuits. 06M

   b) Explain how ATPG tool is selected with an example. 06M

OR

6. a) Discuss about various compression techniques with examples. 06M

   b) Describe the concept of syndrome testing with an example. 06M

UNIT-IV

7. With the help of a neat block diagram, explain about the scan architecture and testing with an example. 12M

OR

8. Describe how the generic boundary scan is performed with relevant examples. 12M

UNIT-V

9. Discuss about the following BIST architectures: 12M

   (a) CSBL (b) BEST (c) LOCST (d) STUMPS

OR

10. With an example, describe the design procedure for self test at board level 12M

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Code: 4PC321

R-14

M. Tech. II-Semester Regular Examinations Oct/Nov 2015

Low Power VLSI Design

(VLSI System Design)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. a) Explain about the Design Limitations imposed on Low-Power, Low-Voltage Circuits Pertaining to the following Parameters.
   i) Power Supply Voltage
   ii) Threshold Voltage
   iii) Scaling
   iv) Interconnect Wires — 8M
   b) What are the advantages and limitations of Silicon-on-Insulator Technology? — 4M

OR

2. a) Draw the diagram of a MOSFET structure with double diffused drain and explain about the same. — 6M
   b) Give the process steps for Retrograde-well MOS structures — 6M

UNIT-II

3. With schematic diagrams explain about deep submicron processes in detail. — 12M

OR

4. a) Discuss about the low capacitance Bipolar/Bi-CMOS deep submicron process. — 6M
   b) Discuss about the Copper interconnects for deep submicron CMOS/Bi-CMOS process in brief. — 6M

UNIT-III

5. a) With the help of equations, describe the Level 1 and Level 2 Models of MOSFET. — 6M
   b) Describe the sub threshold current model of MOSFET. — 6M

OR

6. a) With neat sketches, explain the HSPICE Level 50 MOSFET model in detail. — 6M
   b) Explain Gummel-Poon bipolar spice model with neat sketches. — 6M

UNIT-IV

7. a) Discuss about the characteristics of BiCMOS Circuits utilizing lateral p-n-p BJTs in PMOS structures. — 6M
   b) Explain the performance valuation of Merged BiCMOS logic gates. How the weak points of conventional BiCMOS logic gates are overcome by these circuits? — 6M

OR

8. a) Explain the concept of power dissipation in conventional CMOS logic gates. — 6M
   b) Discuss ESD-free Bi-CMOS digital circuit with a neat diagram and give its advantages. — 6M

UNIT-V

9. a) Explain the optimization theme and performance themes of Latches & Flip-flops. — 6M
   b) Explain the need for low power Latches and Flip-Flops. Give the major uses of Latches and Flip-Flops. — 6M

OR

10. a) Discuss about the Functionality Theme and Synchronous themes of latches and Flip – Flops. — 6M
    b) What are the quality measures for latches and Flip flops? Explain. — 6M

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Code: 4PB323

R-14

M. Tech. II-Semester Regular Examinations Oct/Nov 2015

Hardware Software Co-Design

(Common to Embedded Systems & VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. a) Discuss the languages which are essential used in co-design model 6M
   b) With a flow diagram explain the principle of generic co-design methodology 6M

OR

2. a) Explain briefly, Co-synthesis algorithm which is used for different Models of Software Partitioning 6M
   b) How co-synthesis methods for distributed computing systems are different from single rate design systems? 6M

UNIT-II

3. a) Explain prototyping and emulation Techniques based on hardware, software co-design with examples 6M
   b) What are the Target Architectures and explain with the help of applications 6M

OR

4. Compare Architectures for control dominated systems with data dominated systems in classifying Target architectures for embedded systems. 12M

UNIT-III

5. a) List out the design tools of embedded software development needs of embedded processors and its importance. 6M
   b) Discuss about the Mixed systems and Less specialized systems with Applications 6M

OR

6. Discuss the pragmatic issues in setting up a compiler environment for embedded systems. 12M

UNIT-IV

7. a) Explain briefly, Coordinating concurrent computations classifications 6M
   b) List out the Verification tools and explain its 6M

OR

8. a) Distinguish between System level specification languages with examples 6M
   b) Discuss about System level specification languages with applications 6M

UNIT-V

9. a) Write a short notes on the system level synthesis and its Design 6M
   b) Discuss briefly on the co-design computational model 6M

OR

10. Why different techniques are introduced for heterogeneous specifications and multi-language co-simulation? Discuss. 12M

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Hall Ticket Number :

R-14

Code: 4PC322

M. Tech. II-Semester Regular Examinations Oct/Nov 2015

ASIC Design

(VLSI System Design)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. a) Explain the sequence of steps involved in the design of an ASIC 8M
   b) Illustrate the essential characteristics of an FPGA 4M

OR

2. Discuss different types of Semicustom ASICs 12M

UNIT-II

3. Briefly discuss the concepts involved in the design outline of PLD 12M

OR

4. a) Design the logic schematic for the PAL with a maximum of 22 inputs and 132 product terms 8M
   b) List out the important characteristics of PAL 4M

UNIT-III

5. Explain the characteristics and performance of Gate array ASICs with an example 12M

OR

6. Explain the characteristics and performance of mixed mode and analogue ASICs with an example 12M

UNIT-IV

7. a) Explain the different categories of pre-layout and post-layout simulation checks 6M
   b) Explain the steps involved in the design flow of logic synthesis 6M

OR

8. Discuss how the Verilog Logic synthesis happens in ASICs 12M

UNIT-V

9. a) Write about the iterative placement improvement algorithm 8M
   b) Derive an algorithm for placement of logic cells by applying simulated Annealing 4M

OR

10. a) How the global routing is made in ASICs 8M
    b) What is meant by timing driven detailed routing 4M

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Hall Ticket Number :

Code: 4PC323 **R-14**

M. Tech. II-Semester Regular Examinations Oct/Nov 2015

Algorithms for VLSI Design Automation

(VLSI System Design)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. a) Discuss about tractable and intractable problems 6M
   b) Explain Genetic algorithms in detail. 6M

OR

2. a) Discuss about design automation tools. 6M
   b) Explain Simulated annealing. 6M

UNIT-II

3. a) Explain connectivity modeling. 6M
   b) Explain simulation mechanisms. 6M

OR

4. a) Explain compiler-driven simulation. 6M
   b) Explain switch-level modeling and simulation. 6M

UNIT-III

5. a) Explain ROBDD principles in detail. 6M
   b) Explain two-level logic synthesis. 6M

OR

6. a) Discuss about ROBDD manipulation. 6M
   b) Explain basic issues and terminology of logic synthesis & verification. 6M

UNIT-IV

7. a) Explain data, control, and clocks with respect to hardware models for high level synthesis. 6M
   b) Discuss about data-flow graph representation. 6M

OR

8. a) Explain Mobility based scheduling. 6M
   b) Discuss about Assignment by clique partitioning. 6M

UNIT-V

9. a) Discuss about physical design cycle for FPGA's. 6M
   b) Explain Routing and programmable MCM's. 6M

OR

10. a) Discuss about partitioning and routing for segmented and staggered models. 6M
    b) Explain distribution & routing. 6M

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Hall Ticket Number :

Code: 4PB324

R-14

M. Tech. II-Semester Regular Examinations Oct/Nov 2015

DSP Processors and Architectures

(Common to DECS, Embedded Systems & VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60Marks)

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UNIT-I

1. Explain FFT algorithm for DFT computation with the help of butterfly diagram in detail 12M

OR

2. a) What are the various types of discrete time sequences in DSP for analysis purpose and give their definitions and MATLAB representations 8M

   b) Write Short notes on Compensating filter. 4M

UNIT-II

3. a) Explain Bus architecture & speed issues of programmable DSP devices. 8M

   b) Explain the basic architectural features considered for programmable DSP devices. 4M

OR

4. Describe the sources of error for evaluating the computational accuracy in DSP implementations. 12M

UNIT-III

5. Write a program to implement decimation & interpolation on TMS320C54XX 12M

OR

6. a) Explain the six-levels of pipeline structure of TMS320C54XX processor. 8M

   b) What is Q-notation? How it is used for DSP implementations? 4M

UNIT-IV

7. a) What is the role of anti aliasing and reconstruction filters in DSP system? 8M

   b) Write short notes on FIR and IIR filter in all respects. 4M

OR

8. Explain the features for external interfacing in connection with programmable DSP devices. 12M

UNIT-V

9. a) Explain how to interface the parallel I/O peripherals to programmable DSP devices with suitable example 8M

   b) Explain MCBSP in detail. 4M

OR

10. a) Write about CODEC interfacing circuit with neat sketch. 8M

    b) What are different external bus interfacing signals? In detail. 4M

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