Code: 9A04401

1

II B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2012

SWITCHING THEORY & LOGIC DESIGN

(Common to EEE, EIE, E.Con.E, ECE & ECC)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
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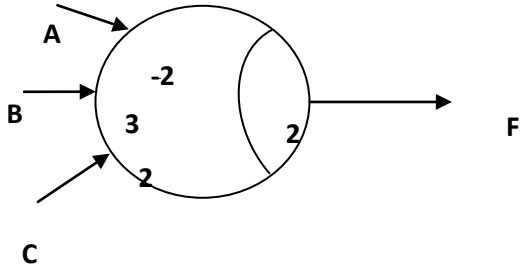
1 (a) What is the necessity of binary codes in computers?
(b) Why the ASCII code was developed? Explain ASCII code with table.
(c) Encode the word DIGITAL in to 7 bit ASCII code.

2 (a) What are universal gates? Realize AND, OR, NOT, XOR gates using universal gates.
(b) Determine the canonical sum of minterms form of the following function. F(W,X,Y,Z) = 1
(c) Prove the Boolean identity X+YZ = (X+Y) (X+Z).

3 (a) What are the advantages of tabulation method over K-map?
(b) Simplify the following Boolean function using tabulation method:
Y(A,B,C,D) = ∑ (0,1,3,7,8,9,11,15).

4 (a) Design a combinational circuit that accepts a three-bit binary number and generates an output binary number equal to the twice the input number.
(b) Design 2*4 decoder using NOR gates.

5 (a) For the figure given below obtain the logic expression for the threshold element and determine its equivalent gate circuit.



(b) What are the capabilities and limitations of T-gate?

6 (a) What is meant by race around condition? Briefly explain.
(b) Explain the operation of synchronous counter.

7 (a) Discuss mealy and Moore machine models of sequential machines.
(b) Explain the minimization procedure for determining the set of equivalent state of a specified machine M.

8 (a) How do you indicate Moore outputs and mealy outputs in an ASM block?
(b) Obtain the ASM chart for the following state transition. Start for State T_1; then if xy=00, go to T_2 if xy=01, go to T_3; if xy=10 go to T_1; otherwise go to T_3.

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Code: 9A04401

2

II B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2012

SWITCHING THEORY & LOGIC DESIGN

(Common to EEE, EIE, E.Con.E, ECE & ECC)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) List the decimal numbers -8 to +7 in sign-magnitude, sign-1's complement and sign-2's complement representation and conclude the advantage of 2's complement representation in computers.

(b) What is the advantage of 2's complement representation in computers? Perform the following operations using 2's complement method: (i) (+55) – (+15) (ii) (-55) – (-15)

2 (a) State and prove De Morgan's laws. Mention gate equivalents.

(b) Determine the canonical sum of products form of the following function:
f (x, y, z) = z + (x'+ y)(x + y').

(c) Realize XOR gate using minimum number of NAND gates.

3 Simplify the following Boolean expressions using K-map and implement them using NOR gates: (i) F (A, B, C, D) = AB'C' + AC + A'CD'.
(ii) F (W, X, Y, Z) = W'X'Y'Z' + WXY'Z' + W'X'YZ + WXYZ.

4 A combinational circuit has four inputs and one output. The output is equal to 1 when
(i) all the inputs are equal to 1 or
(ii) none of the inputs are equal to 1 or
(iii) when even number of inputs are equal to 1
Design the above circuit using logic gates.

5 Program a 3 input and 4 output PLA Circuit to implemented the sum and carry outputs of a full adder.

6 (a) Show how mod-12 JK counter could be built using mod-3 & mod-4 counters.

(b) Explain the steps in synchronous sequential circuit design.

7 Explain the following related to sequential circuits with suitable examples.
(a) State diagram.
(b) State table.
(c) State assignment.

8 (a) Explain the symbols used in an ASM chart with neat diagrams.

(b) Explain the important features of the ASM chart.

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Code: 9A04401

3

II B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2012

SWITCHING THEORY & LOGIC DESIGN

(Common to EEE, EIE, E.Con.E, ECE & ECC)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) List the binary, octal and hexa numbers for decimal 16 to 31.
(b) Perform the following operations using 2's complement method: (i) 48 – 23 (ii) 23 – 48.

2 (a) State and prove Boolean laws related to OR, AND, NOT gates.
(b) Given Boolean expression AB'+A'B = C. Show that AC'+A'C = B.
(c) Prove that OR-AND network is equivalent to NOR-NOR network.

3 (a) Simplify the following Boolean function for minimal SOP form using K-map
$F(W,X,Y,Z) = \sum(0,1,2,3,4,6,8,9,10,11)$
(b) Simplify the following Boolean functions using K-map.
(i) F(A,B,C) = A'B + B'C + A'B'C' (ii) F(A,B,C) = A'B' + AC' + B'C + A'BC'

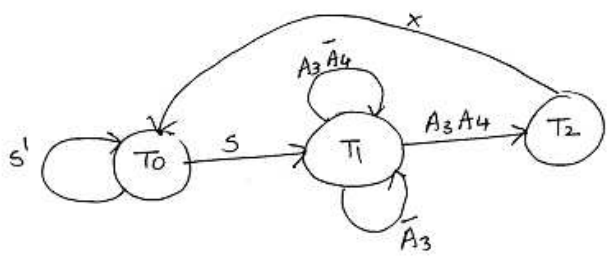
4 (a) Implement full adder using 4*1 multiplexer.
(b) Design 4*16 decoder using two 3*8 decoders with block diagram.

5 (a) Explain the general combinational PLD configuration with suitable block diagram.
(b) Give the logic implementation of a 32 x 4 bit & 8 x 4 bit ROM using suitable decoder.

6 (a) Draw the circuit diagram of 4 bit ring counter using D flip flops and explain its operation with the help of bit pattern.
(b) Distinguish between transition table and excitation table.

7 A clocked sequential circuit with simple input x and single output Z produce an output Z = 1 whenever the input x completes the sequence 1 0 1 1 and overlapping is allowed.
(a) Obtain its state - diagram.
(b) Obtain its minimal state - table and design the circuit with D - Flip-Flops.

8 (a) For the given control state diagram obtain its equivalent ASM chart.
(b) Design control logic circuit using multiplexers for the given state diagram.



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Code: 9A04401 4

II B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2012

SWITCHING THEORY & LOGIC DESIGN

(Common to EEE, EIE, E.Con.E, ECE & ECC)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) Why the computer hardware works for binary number system? List the binary, octal and hexa numbers for decimal 0 to 15.
(b) Given a = 10101001 and b = 1101. Find: (i) a + b (ii) a – b (iii) a. b (iv) a / b.

2 (a) Draw the symbols and truth tables of all logic gates and explain.
(b) Simplify the following Boolean functions to a minimum number of literals:
(i) x + x'y (ii) x (x' +y) (iii) x'y'z + x'yz + xy' (iv) xy + x'z +yz.

3 (a) What are don't-care conditions? Explain its advantage with example.
(b) Simplify the following Boolean function for minimal SOP form using K-map and implement using NAND gates. $F(W,X,Y,Z) = \sum(1,3,7,11,15) + d(0,2,5)$.

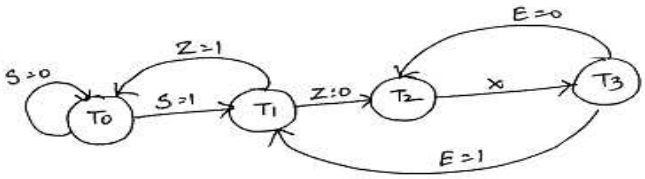
4 (a) What is decoder? Construct 3*8 decoder using logic gates and truth table.
(b) What is encoder? Design octal to binary encoder.

5 (a) Explain the internal structure of PLA.
(b) Design a full adder circuit using ROM.

6 (a) What are asynchronous inputs in flip flops? Explain its functionality.
(b) With neat sketch explain JK master slave flip flop.

7 (a) Write the differences between Mealy and Moore type machines.
(b) A sequential circuit has 2 inputs w_1=w_2 and an output z. Its function is to compare the input sequence on the two inputs. If w_1=w_2 during any four consecutive clock cycles, the circuit produces z=1 otherwise z=0.
w_1 = 0110111000110 w_2 = 1110101000111 z = 0000100001110

8 (a) For the given control state diagram obtain its ASM chart.
(b) Design the circuit.



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Code: 9A04402

1

II B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2012

ELECTRONIC CIRCUIT ANALYSIS

(Common to EIE, E. Con. E & ECE)

Time: 3 hours Max Marks: 70

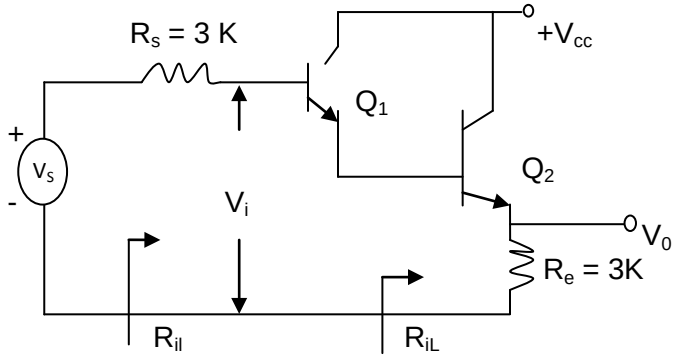
Answer any FIVE questions
All questions carry equal marks
*****

1 (a) Draw the circuit of an emitter follower and its equivalent circuit. List out its characteristics.

(b) The h-parameters of the transistor used in CE amplifier are h_{fe} = 50, h_{ie} = 1.1KΩ, h_{re} = 2.5 x 10^{-4}, h_{oe} = 24 μA/V. Find out current gain and voltage gain with and without source resistance, input and output impedances, given that R_L = 10 K and R_s = 1 K.

2 (a) Draw the circuit diagram of cascade amplifier with and without biasing circuit. What are the advantages of this?

(b) For the circuit shown in figure, calculate R_i, A_i, A_v and R_o. Assume h_{ie} = 1.1 K, h_{fe} = 50, h_{re} = 2.5 x 10^{-4}, h_{oe} = 25 μA/v.



3 (a) Draw hybrid – π model for a transistor in the CE configuration and explain the significance of every component in this model.

(b) A HF amplifier uses a transistor which is driven from a source with R_s = 1 K. Calculate value voltage gain, gain bandwidth product, upper 3 dB cut off frequency f_H, if R_L = 0 and R_L = 2 K. Typical values for hybrid – π parameters are: $r_{b'e}$ = 1 K, rbb^1 = 100 ohms, c_e = 100 PF. C_c = 3 PF and g_m = 50 mA/v.

4 (a) Discuss using the concept of a load line superimposed on the transistor characteristics, how a simple common source circuit can amplify a time varying signal.

(b) Determine the small signal voltage gain and input and output resistances of a common source amplifier. For the circuit shown in figure the parameters are: V_{DD} = 10 V, R_1 = 70.9 KΩ, R_2 = 29.1 KΩ and R_D = 5 KΩ. The transistor parameters are: V_{TN} = 1.5 V, K_n = 0.5 mA/V^2 and λ = 0.01 V^{-1}. Assume R_{si} = 4 KΩ. See figure (no.4) in the next page.

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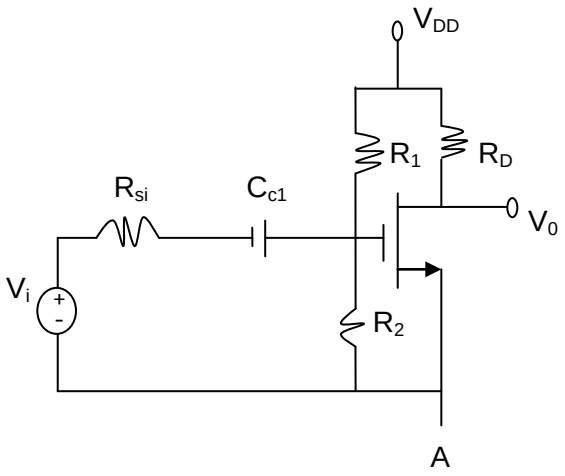

Figure 4

5 (a) Discuss the effects of negative feedback on frequency response of an amplifier.

(b) An amplifier with an open loop voltage gain of 1000 delivers 10 W of power output at 10% harmonic distortion when input is 10 mV. If 40 dB negative feedback is applied and output power is to remain at 10 W, determine required input signal V_s and second harmonic distortion with feedback.

6 (a) What type of feedback is employed in oscillators and what are the advantages? Discuss the conditions for sustained oscillations.

(b) Discuss and explain the basic circuit of an LC oscillator and derive the condition for the oscillations.

(c) A crystal has l = 0.1 H, C = 0.01 PF, R = 2 Ω and C $_M$ = 1 PF. Find the series resonance and Q-factor.

7 (a) Draw a practical circuit of a complimentary symmetry push pull amplifier circuit. Explain its function.

(b) State the expression relating the total output power ‘P’; total harmonic distortion ‘D’ and the fundamental power ‘P’ in power amplifiers. If total distortion in the amplifier is 9%; calculate its contribution to the total power.

8 (a) Explain the working of a single tuned amplifier. Draw its frequency response.

(b) Derive the equation for the 3 dB band width of capacitance coupled single tuned amplifier.

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Code: 9A04402

2

II B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2012

ELECTRONIC CIRCUIT ANALYSIS

(Common to EIE, E. Con. E & ECE)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) Design a single stage emitter follower having R_i = 500 KΩ and R_o = 20 Ω. Assume h_{fe} = 50, h_{ie} = 1 K, h_{oe} = 25 μ A/V.

(b) For a single stage transistor amplifier, R_s = 5K and R_L = 10 K. The h-parameter values are h_{fe} = 50, h_{ie} = 1.1 KΩ, h_{re} = 2.5 x 10^{-4}, h_{oe} = 25μA/V. Find A_I, A_v, A_{vs}, R_i and R_o for the CE transistor configuration.

2 (a) Compare emitter follower and Darlington emitter follower configurations in respect of:
(i) Current gain. (ii) Input impedance
(iii) Voltage gain (iv) Output impedance.

(b) If four identical amplifiers are cascaded each having f_L = 100 Hz, determine the overall lower 3 dB frequency. Assume non interacting stages.

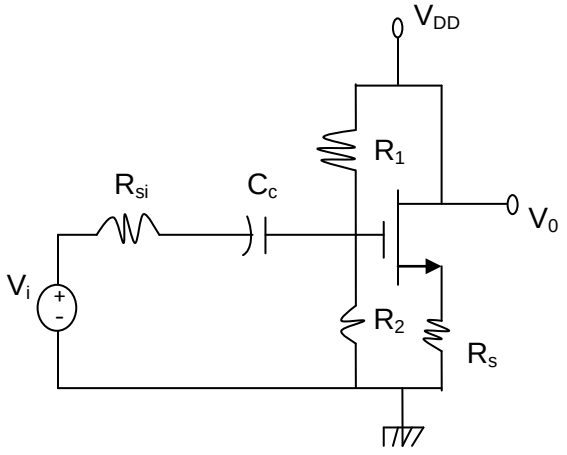
(c) Write a short note on Gain-Band width product of amplifiers.

3 (a) Derive the expressions for trans-conductance and input conductance of CE amplifier using HF model.

(b) The LF parameters of a transistor at I_c = 20 mA, V_{ce} = 10 V and at room temperature h_{ie} = 400, h_{oe} =10^{-5} A/V, h_{fe} = 150, h_{re} = 10^{-4}. At the same operating point f_T = 60 MHz and C_{ob} = 3 PF, compute the values of the entire hybrid – π parameters.

4 (a) Sketch a simple common drain amplifier circuit and discuss general ac circuit characteristics.

(b) Calculate the small signal voltage gain of the source follower circuit shown in figure. Assume the circuit parameters are V_{DD} = 12V, R_1 = 162 KΩ, R_2 = 463 KΩ and R_s = 0.75 KΩ. The transistor parameters are: V_{TN} = 1.5 V, K_n = 4 mA/V^2 and λ = 0.01 V^{-1}. Assume R_{si} = 4 KΩ.



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5 (a) A voltage series negative feedback amplifier has a voltage gain without feedback of A = 500, input resistance R_i = 3 K, output resistance R_o = 20 K and feedback ratio β = 0.01. Calculate the voltage gain, input resistance and output resistance of the amplifier with feedback.

(b) An amplifier has mid band gain of 125 and a bandwidth of 250 KHz.
(i) If 4% negative feedback is introduced, find the new bandwidth and gain.
(ii) If bandwidth is restricted to 1MHz, find the feedback ratio.

6 (a) What are the factors that affect the frequency stability of an oscillator? How frequency stability can be improved in oscillators?

(b) Find c and h_{fe} of a transistor to provide f_o of 50 KH_Z of an Rc phase shift oscillator, given R_1 = 22 kΩ, R_2 = 68 kΩ, R_c = 20 kΩ, R = 6.8 kΩ and h_{ie} = 2 kΩ.

(c) What is piezoelectric effect? Explain the working of crystal oscillator.

7 (a) Distinguish between large signal and small signal amplifiers.

(b) Compare the series fed and transformer coupled class – A power amplifiers. Why is the conversion efficiency doubled in transformer coupled class – A amplifier?

8 (a) Explain as to how you can increase the selectivity of single tuned amplifier. Draw the circuit diagram and explain its operation and also draw its frequency response.

(b) What is a stagger tuned amplifier and explain its working?

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Code: 9A04402

3

II B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2012

ELECTRONIC CIRCUIT ANALYSIS

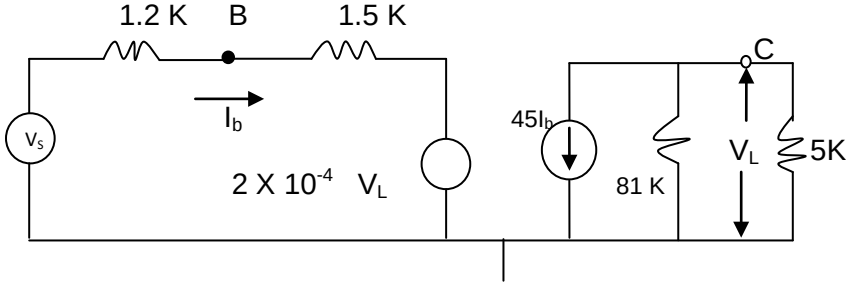
(Common to EIE, E. Con. E & ECE)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

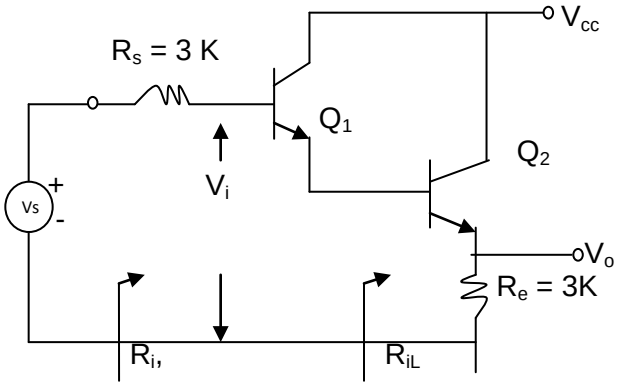
1 (a) For a single stage transistor amplifier, R_s = 10 K and R_L = 10 K. The h-parameter values are h_{fc} = -51, h_{ic} = 1.1 KΩ, h_{rc} = 1, h_{oc} = 25μA/V. Find A_I, A_V, A_{VS}, R_i and R_o for the CC transistor configuration.

(b) The small signal h-parameter ac equivalent circuit of a certain transistor connected in CE configuration is shown in figure. Calculate current gain, voltage gain, input impedance and output impedance by deriving the expressions for the above.



2 (a) Discuss the effect of emitter bypass capacitor and input & output coupling capacitors on the lower cut-off frequency if number of amplifiers is cascaded.

(b) For the circuit shown in figure, calculate R_i, A_i, A_v and R_o. Assume h_{ie} = 1.1 K, h_{fe} =50, h_{re} =2.5 x 10^{-4}, h_{oe} = 25μ A/v.



3 (a) Define f_α, f_β and f_T and derive the relation between f_β and f_T.

(b) Derive all components in the hybrid – π model in terms of h parameters in CE configuration.

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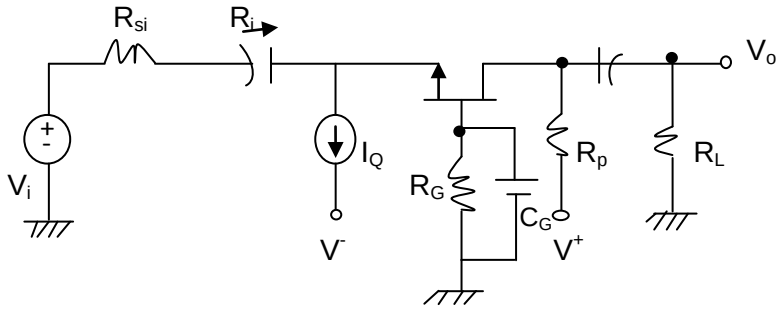
4 (a) Sketch a simple common gate amplifier circuit and discuss the general ac characteristics.

(b) For the circuit shown in figure, determine the output voltage for a given input current. The circuit parameters are: I_Q = 1MA, V^+ = 5V, V^- = -5V, R_G = 100 KΩ, R_D = 4 KΩ and R_L = 10 KΩ. The transistor parameters are: V_{TN} = 1 V, K_n = 1m A/V^2 AND λ = 0. Assume the input current is 100 sin wt μA and assume R_{si} = 50 KΩ.



5 (a) Explain the concept of feedback with block diagram.

(b) Define desensitivity. For large values of D, what is Af? What is the significance of this result?

(c) An amplifier has a voltage gain of 400, f_1 = 50 Hz, f_2 = 200 KHz and a distortion of 10 % without feedback. Determine the voltage gain f1f, f2f and Df when a negative feedback is applied with feedback ratio of 0.001.

6 (a) Classify different types of oscillators based on frequency range.

(b) Why RC oscillators are not suitable for high frequency applications?

(c) Show that the gain of Wien bridge oscillator using BJT amplifier must be atleast 3 for the oscillations to occur.

7 (a) A transistor in a transformer coupled (class – A) power amplifier has to deliver a maximum of 5 W to a load of 4 Ω load. The quiescent point is adjusted for symmetrical swing, and the collector supply voltage is V_{cc} = 20 volts. Assume V min = 0 volts:

(i) What is the transformer turns ratio?

(ii) What is the peak collector current?

(b) What is cross over distortion? How can a class – AB power amplifiers avoid cross-over distortion?

(c) What are the advantages and disadvantages of push pull configuration? Show that in class –B push pull amplifier the maximum conversion efficiency is 78.5%.

8 (a) Explain in detail how do you alter the bandwidth of an RF amplifier which is:
(i) Single tuned. (ii) Double tuned (iii) Stagger tuned.

(b) Explain the operation of a double tuned amplifier. Explain the advantages of double tuned circuit over single tuned circuit.

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Code: 9A04402

4

II B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2012

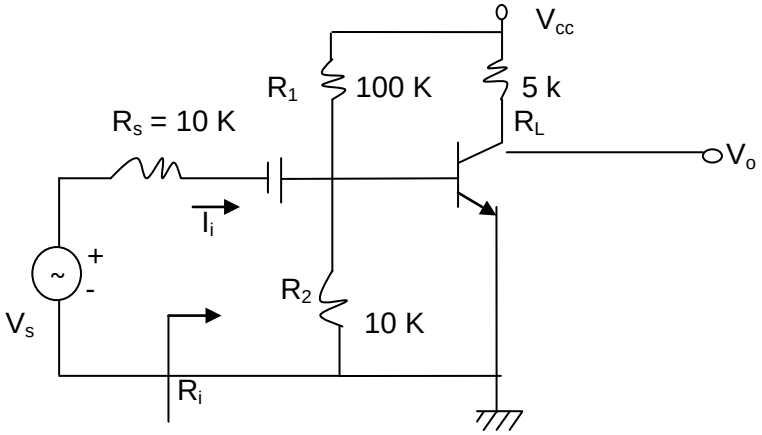
ELECTRONIC CIRCUIT ANALYSIS

(Common to EIE, E. Con. E & ECE)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

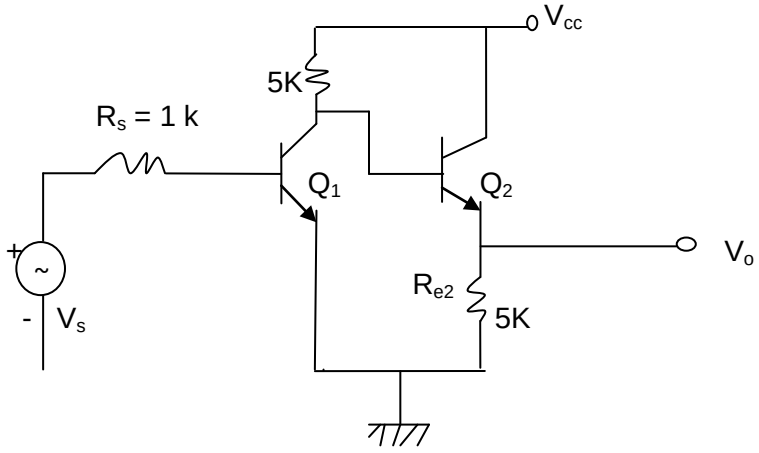
1 (a) The h-parameters of a transistor are h_{fe} = 50, h_{ie} = 1.1 KΩ, h_{re} = 2.5 x 10^{-4}, h_{oe} = 24 µA/V. Calculate A_I, A_V, A_{VS}, R_i and R_o shown in figure.



(b) List out the characteristics of CB amplifier and mention their typical values. Draw the basic CB amplifier circuit and its equivalent h-parameter model. Derive an expression for its R_i and R_o.

2 (a) How multistage amplifiers are classified depending upon the type of coupling?

(b) A two-stage amplifier circuit (CE – CC configuration) is shown in figure. The h-parameter values are h_{fe} = 50, h_{ie} =2 KΩ, h_{re} = 6 x10^{-4}, h_{oe} = 25 µA/V. h_{fe} = -51, h_{ic} = 2 KΩ, h_{rc} =1, h_{oc} = 25 µ A/V. Find the input and output impedances and individual, as well as overall voltage and current gains.



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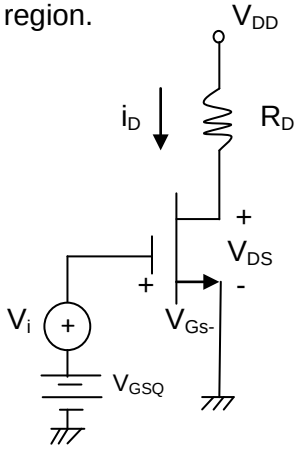
3 (a) Draw hybrid – π model for a transistor in the CE configuration and explain the significance of every component in this model.

(b) Draw the small signal equivalent circuit for an emitter follower stage at high frequencies. Derive expression for voltage gain.

4 (a) Compare the ac characteristics of the common source, source follower and common gate circuits.

(b) Determine the small signal voltage gain of a MOSFET circuit. For the circuit shown in figure, the parameters are: V_{GSQ}= 2.12 V, V_{DD} = 5 V, R_D = 2.5 KΩ. The transistor parameters V_{TN} = 1 V, K_n = 0.8 mA/V^2 and λ = 0.02 V^{-1}. Assume the transistor is biased in the saturation region.



5 (a) What are the different types of negative feedback? Briefly explain how the input and output impedances of an amplifier are affected by the different types of negative feedback.

(b) An amplifier has a voltage gain of 400, f_1 = 50 Hz, f_2 = 200 KHz and a distortion of 10% without feedback. Determine the voltage gain, f_{1f}, f_{2f} and D_f when a negative feedback is applied with feedback ratio of 0.001.

6 (a) Draw the circuit diagram of a RC phases shift oscillator using BJT. Derive the expression for frequency of oscillators.

(b) In a transistorized Hartley oscillator the two inductances are 2 mH and 20 µH while the frequency is to be changed from 950 KH_Z to 2050 KH_Z. Calculate the range over which the capacitor is to be vaired.

7 (a) Derive the expression for maximum collector power dissipation Pc (max) in the case of class B power amplifiers.

(b) Derive the expression, with necessary diagrams, to calculate the total harmonic distortion 'D' in power amplifiers using the five-point method of analysis.

8 (a) Why do we use tuned amplifiers in the IF and RF range?

(b) Derive the expression for bandwidth in terms of resonant frequency and quality factor in case of double tuned amplifiers.

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II B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2012

PULSE & DIGITAL CIRCUITS

(Common to EIE, E.Con.E, ECE,ECC, & MCT)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) Three low pass RC circuits are in cascade and isolated from one another by ideal buffer amplifiers. Find the expression for the output voltage as a function of time if the input is a step voltage.
(b) Find the rise time of the output in terms of RC in the above case.

2 (a) State and prove clamping theorem.
(b) Plot the transfer characteristics of the circuit shown below. Assume ideal diodes.

3 (a) Explain the various switching times involved in transistor. How do you justify that transistor acts as switch?
(b) Describe the breakdown in diodes in detail.

4 (a) Design a collector coupled transistor monostable multivibrator to produce a time delay of 100 μ sec. Use transistors have h_{FE} of 250. Use ±12 v sources, V_{CE}(sat) = 0.3 v, V_{BE}(sat) = 0.7 v and V_{BE} cutoff = 0v.
(b) Show that the astable multivibrator works as voltage controlled oscillator.

5 (a) Define sweep speed, sweep error, sweep duration and sweep types.
(b) For an ideal voltage sweep using ideal current source and ideal switch following data are available. Iconst = 1ma, C = 1 μf. Voltage level of ideal voltage operated switch is 5 volts. Calculate: (a) sweep speed and (b) sweep duration.

6 Clearly explain the concept of synchronization and a synchronization related to the methods of all types of sweep circuits.

7 (a) What is the difference between synchronization on one to one basis and two to one basis?
(b) Describe sine wave frequency division with a sweep circuit.

8 (a) What are the advantages of ICs over discrete components?
(b) Realize AND, OR and NOT gates using diodes.

*****

Code: 9A04404

2

II B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2012

PULSE & DIGITAL CIRCUITS

(Common to EIE, E.Con.E, ECE,ECC, & MCT)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 Explain how RC circuits are used as integrators and differentiators. Sketch the output waveform for square wave input. A pulse of 5 v amplitude and pulse width 0.5 m sec is applied to high pass RC circuit consisting of R = 22 kΩ and C = 0.47 μf. Determine the % tilt in the output waveform.

2 (a) What is meant by clipping in wave shaping?
(b) Classify different types of clipper circuits. Give their circuits and explain their operation with the aid of transfer characteristics.

3 (a) Write short notes on:
(a) Diode switching times. (b) Switching characteristics of transistor.
(b) Explain the phenomenon of latching in a transistor.

4 (a) Explain about the response of Schmitt binary to an arbitrary input signal with appropriate diagram.
(b) Explain how Schmitt trigger can be used as a comparator and as a squaring circuit.

5 (a) Why bootstrap time base generator is called so?
(b) What are the various methods of generating sweep voltage? Explain.

6 (a) Explain the differences between four diode gates and six diode gates.
(b) Explain clearly about alternate form of four diode gate.

7 (a) Explain the generation of saw tooth waveform using RC sweep circuits.
(b) What are the factors that affect the phase delay?

8 (a) Explain with neat diagram the operation of DTL NOR gate.
(b) Write about propagation delay in logic families.

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Code: 9A04404

3

II B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2012

PULSE & DIGITAL CIRCUITS

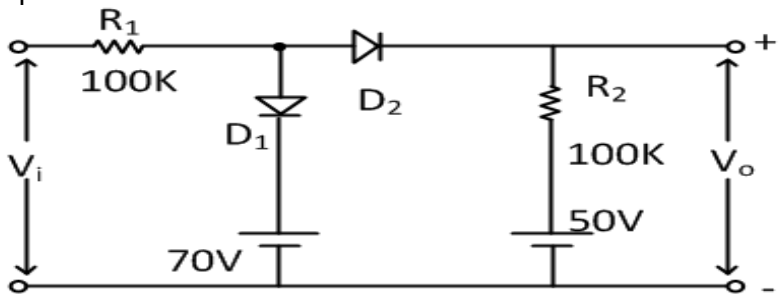
(Common to EIE, E.Con.E, ECE,ECC, & MCT)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) Obtain the response of RC high pass circuit for an exponential i/p signal
(b) A square wave, whose peak-to-peak valve is I V, extends I0.5 V w.r.t. to ground. The half period is O.1 sec this voltage impressed upon an RC differentiating circuit whose time constant is 0.2 sec. Determine the maximum and minimum valves of the l/p voltages in the steady state.

2 (a) With the help of neat circuit explain the working of negative clamping circuit. What is the effect of Rs & Rf is clamping circuit output?
(b) The input voltage of the two level clipper is varying linearly from 0 to 80 V. Draw the output waveform and transfer characteristics.



3 Explain how a BJT can be used as a switch. Compare its performance as a switch with JFET. Explain all switching times.

4 (a) Derive an expression for the period of oscillations of astable multivibrator.
(b) Bring out the effect of supply voltage, junction voltages and temperature on the period of oscillations of the astable multivibrator.

5 What are the techniques used to improve the linearity of current sweeps? Illustrate with examples.

6 Describe the errors encountered in series sampling and what is the elaborate design procedure that is adopted to minimize these errors.

7 (a) Discuss about triggering methods used in multivibrator circuits.
(b) How astable multivibrator can be synchronized?

8 (a) Explain the operation of a NAND gate with the help of a circuit diagram.
(b) Explain IC packaging techniques.

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Code: 9A04404

4

II B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2012

PULSE & DIGITAL CIRCUITS

(Common to EIE, E.Con.E, ECE,ECC, & MCT)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) Explain about RLC ringing circuit.
(b) Explain RC double differentiator circuit.

2 (a) What is meant by clipping in wave shaping?
(b) Classify different types of clipper circuits. Give their circuits and explain their operation with the aid of transfer characteristics.

3 (a) Explain Piecewise linear characteristics of diode.
(b) Discuss in detail about transistor switching times.

4 (a) Draw the circuit diagram of Schmitt trigger and explain its operation. Derive the expression for UTP and LTP.
(b) Discuss the various methods of triggering a multivibrator.

5 (a) Explain the operation of bootstrap time base generators.
(b) Explain various methods to achieve a linear sweep waveform.

6 Sketch circuit of simple diode bidirectional sampling gate and describe its function with waveforms. Obtain expressions for gain and control voltages.

7 (a) Explain about several factors that affect phase delay.
(b) What is the condition to be met for pulse synchronization?

8 (a) Compare current spikes in ECL and TTL gates.
(b) What happens if output accidentally gets shorted to ground in CMOS and NMOS?

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Code: 9A04406

II B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2012

ELECTROMAGNETIC THEORY & TRANSMISSION LINES

(Electronics & Communication Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) Define del operator and hence explain the physical interpretation of the operations gradient, divergence and curl.
(b) State Coulomb's law and derive an expression for electric field at a point.

2 (a) Explain with the help of an example how Poisson's and Laplace equations are used to solve the electromagnetic problems.
(b) Determine the capacitance of a charged sphere of radius 'R'.

3 (a) Discuss the definition of magnetic field intensity and permeability concept.
(b) What is magnetic flux density? How is it defined in terms of force on a current element?

4 (a) Give the word statements of Maxwell's equations.
(b) In a conducting medium do the static electric and magnetic fields both exist. Explain.

5 Obtain the relation between E & H in uniform plane wave and obtain the characteristic impedance of the non conducting medium.

6 (a) Explain about direction cosines.
(b) A uniform plane wave in air is reflected from the surface of material whose properties are unknown. Measurements of electric field is the region in front of the interface yield a 1.5 m spacing between maximum, with first maximum occurring at 0.75 m from the interface. Standing wave ratios of 5 is measured then find intrinsic impedance of the unknown material.

7 Explain the measurement of inductance and loop resistance for open wire line and coaxial cable.

8 What is Smith chart? Derive the equations for constant resistance and constant reactance circles.

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Code: 9A04406

2

II B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2012

ELECTROMAGNETIC THEORY & TRANSMISSION LINES

(Electronics & Communication Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) Write about different types of charge distributions.
(b) Derive an expression for the electric field due to infinite plane sheet of uniform surface charge.

2 (a) What is uniqueness theorem? Prove it with respect to static fields.
(b) Determine the energy stored in order to distribute charge on concentric spherical shell.

3 (a) Explain the concept of scalar magnetic potential and hence define magneto motive force.
(b) Find the magnetic vector potential due to an infinite plane current sheet of uniform density 'K'.

4 Give the expressions for Maxwell's equations for static fields and hence derive the modifications made in these equations for time varying fields.

5 Determine the phase velocity of propagation, attenuation constant, phase constant and intrinsic impedance for a forward traveling wave in a large block of copper at 1 MHz ($\sigma = 5.8 \times 10^7$, $\epsilon_r = 1$and $\mu_r = 1$). Determine phase shift between the electric and magnetic fields and the distance that the wave must travel to be attenuated by a factor of 100 (40 db).

6 Explain reflection of uniform plane wave by a perfect dielectric in the case of normal incidence and obtain the expressions for reflection and transmission coefficients.

7 The propagation constant and characteristic impedance of a line of length l are given by γ and Z_0 respectively, find its equivalent T network.

8 (a) Discuss in detail about impedance matching.
(b) The characteristic impedance of the line R_0 is 50 Ω, and the SWR $\rho = 2$ when the line is loaded. When the line is shorted, the minima shift 0.15 λ toward the load. Determine the load impedance.

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Code: 9A04406

3

II B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2012

ELECTROMAGNETIC THEORY & TRANSMISSION LINES

(Electronics & Communication Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 Define the term electric potential in electrostatic field. Show that the potential difference between any two points is independent of path of integration.

2 Explain briefly the electric field 'E' and electric flux density 'D' and permittivity concept in a dielectric material when subjected to external field.

3 (a) Find the magnetic field due to a circular loop carrying current '**I**' at a distant point from the loop.
(b) Find the flux density at a point due to a long filamentary conductor carrying a current of 20 Amps in **z**- direction.

4 State and prove the boundary conditions for time varying fields. Do they differ for static fields. Explain.

5 Determine the relation between α, and β such that $E = E_m \sin \alpha x \cos (\omega t - \beta z)$ ay satisfies the wave equation in loss less medium.

6 State and prove Poynting theorem.

7 (a) Discuss about primary and secondary constants of the line.
(b) Explain measurement of primary constants experimentally.

8 (a) Explain why short circuited sections are preferable to open circuited sections.
(b) Calculate the length of a piece of 50 Ω open circuited line if its input admittance is to be $j\ 80 \times 10^{-3}$ s.

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Code: 9A04406

4

II B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2012

ELECTROMAGNETIC THEORY & TRANSMISSION LINES

(Electronics & Communication Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) Find the work done in moving a test charge by an infinitesimal distance in an electric field. What amount of work is done in moving it normal to the electric field?
(b) Discuss the formation of surface charge at the boundaries of a conductor placed in static electric field.

2 Describe the phenomenon of polarization and hence discuss the effect of polarization in dielectric materials.

3 (a) Explain in detail the Ampere's law of force.
(b) Two identical circular loops each carrying current of 100 Amps are placed at a distance of 0.01 m. Find the force of attraction / repulsion between them.

4 (a) Discuss in detail the common analogies of electric and magnetic fields.
(b) Region between the two coaxial cones has a potential V_1 at $\boldsymbol{\theta}_1$ (edge of inner cone) and V= 0 at $\boldsymbol{\theta}_2$ (edge of outer cone). The cone vertices are insulated at r = 0. Solve Laplace's equation to get potential at a cone at any angle $\boldsymbol{\theta}$.

5 (a) Dry ground has a conductivity of 5×10^{-4} mhos/m and a relative dielectric constant of 10 at a frequency of 500 MHz. Compute: (i) the intrinsic impedance (ii) the propagation constant (iii) the phase velocity.
(b) Copper has a conductivity of 5.8×10^{7} mhos/m and is considered an ideal material for shielding. A shield is made of copper with a thickness of 1 mm. If a uniform plane wave is incident on the copper shield, compute the absorption loss in decibels by the copper at f = 10 MHz.

6 Explain about instantaneous, average, and complex Poynting vectors.

7 Explain in detail about different types of loading.

8 (a) Describe the procedure for locating the voltage maxima and minima on transmission line and derive the relevant equations.
(b) A 70 Ω lossless line has s =1.6 and $\theta = 300^0$. If the line is 0.6 λ long, calculate the distance of the first minimum voltage from the load.

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Code: 9AHS401

1

II B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2012

MANAGERIAL ECONOMICS & FINANCIAL ANALYSIS

(Common to EIE, E. Con. E & ECE)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) Define managerial economics. Explain its scope.
(b) Distinguish between economics and managerial economics with suitable examples.

2 What do you understand by 'Elasticity of Demand'? What are the types of elasticity of demand?

3 What are the economies of scale? Explain different types of internal and external economies of scale.

4 Define market. Explain any four methods of pricing, based on strategy.

5 Define joint stock companies. Explain its features, advantages and limitations.

6 (a) What is the importance of capital?
(b) What factors determine the working capital requirements of a company?

7 (a) Define accounting and explain its functions.
(b) Explain classification of accounts with suitable examples.

8 Discuss the importance of ratio analysis for inter firm and intra-firm comparison, including circumstances responsible for its limitations, if any?

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Code: 9AHS401

2

II B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2012

MANAGERIAL ECONOMICS & FINANCIAL ANALYSIS

(Common to EIE, E. Con. E & ECE)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 With the following information compute:
(a) Current ratio (b) Quick ratio (c) Stock turnover ratio (d) Gross profit ratio

	Rs.		Rs.
Opening stock	1,00,000	Cash on hand	3,00,000
Closing stock	2,00,000	Debtors	4,00,000
Purchases	5,45,000	Sundry creditors	3,00,000
Wages	15,000	Bills payable	2,50,000
Administrative expenses	4,000	Bank credit	2,50,000
Selling and distribution expenses	2,40,000		
Sales	10,00,000		

2 (a) Define partnership and explain its silent features and limitations**.**
(b) What are the qualities of a good partner?

3 Define 'Accounting Rate of Return' and Payback Period Method'? Compare and contrast the two. Illustrate with assumed data.

4 (a) Explain the main objectives of accounting and its important functions.
(b) Define income statements, and explain its importance.

5 State and explain the law of demand. What are its exceptions?

6 Define elasticity of demand. Explain its types and significance.

7 Draw total product, average product and marginal product curves on your answer book. Explain how output changes with fixed capital and variable labour inputs.

8 Define market. Distinguish between perfect and imperfect markets.

*****

Code: 9AHS401

3

II B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2012

MANAGERIAL ECONOMICS & FINANCIAL ANALYSIS

(Common to EIE, E. Con. E & ECE)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 Define demand. What are its determinants and demand curve?

2 What are the steps in scientific approach to demand forecasting?

3 (a) Explain how you determine BEP through a graph.
(b) A lathe workshop owner uses 1500 units of certain spare part. He buys this from the market for Rs.250. The same can be manufactured in his workshop with a fixed cost of Rs.40,000 and a variable cost of Rs.500. Do you suggest him to make or buy from the market? It is possible that he can sell 5000 units of the same spare part to other lathe shops in the town.

4 What is a market? Explain, in brief, the different market structures.

5 'Small is beautiful'. Do you think this is the reason for the survival of the sole trader form of business organization? Support your answer with suitable example.

6 The cost of a project is Rs.50,000 and has an expected life of 5 years. The cash inflows for the five years are Rs.24,000, Rs.26,000, Rs.20,000, Rs.17,000, and Rs.16,000 respectively**.**
(a) Determine the payback period. (b) What is the accounting rate of return?

7 Journalize the following transaction in the books of Raja Shekhar:

2005		Rs.
Jan.1	Bought goods from Rao	5000
Jan.2	Sold goods for cash	1500
Jan.5	Sold goods to Murthy	3000
Jan.12	Bought goods for cash	7500
Jan.18	Bought furniture for cash	2000
Jan.20	Discount allowed	2500
Jan.24	Received from Murthy on account	1750
Jan.28	Paid Rao on account	2250
Jan.30	Paid salaries	1500
Jan.31	Paid landlord rent	450

8 What are the purpose and limitations of ratio analysis?

*****

Code: 9AHS401

II B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2012

MANAGERIAL ECONOMICS & FINANCIAL ANALYSIS

(Common to EIE, E. Con. E & ECE)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 One man control is the best in the world, if that one man is big enough to manage everything'. Explain the statement.

2 (a) Define capital budgeting. Explain its importance.
(b) How is useful of payback period method? Explain its features and limitations.

3 The following is the balance sheet of Sri Anurag Enterprises as on 31st Dec 20007.

Liabilities	Rs.	***Assets***	Rs.
Share capital	2,00,000	Buildings	2,00,000
Reserve fund	50,000	Machinery	1,50,000
Profit balance	30,500	Stock on hand	1,00,000
Bank loan	1,50,000	Sundry debtors	60,000
Sundry creditors	70,000	Cash on hand	20,500
Provision for tax	30,000		
	5,30,000		5,30,000

You are required to comment on liquidity and solvency position of the concern.

4 (a) What is 'Journal Entry' and describes its importance in account books?
(b) Explain the basic accounting concepts and convention, Give examples.

5 Elaborate the importance of managerial economics in decision making.

6 What do you understand by demand forecasting? What is the need for it?

7 Write short notes on any two of the following:
a) Margin of safety (b) Assumptions of BEA (c) Contribution.

8 Define monopoly. How is price determined under monopoly?

*****

Code: 9A02401

1

II B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2012

PRINCIPLES OF ELECTRICAL ENGINEERING

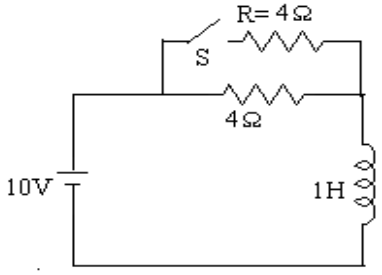
(Common to EIE, E. Con. E, ECE & ECC)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) Show that current in a series RL circuit exited by a dc source of voltage V is I = V/R $(1-e^{-(R/L)t})$ A.

(b) In the above circuit shown in the fig 'S' is open for a long time so that steady state is reached and at t = 0, S is closed. Determine the current i (t) in R = 4 Ω's by using Laplace transform method.



2 (a) Define and obtain open circuit impedance parameters by taking any one example.

(b) A two port network has the following parameters: Z_{11}=20 Ω, Z_{12} = 5 Ω, Z_{21}= 20 Ω and Z_{22}= 15 Ω. Calculate Short circuit parameters.

3 Design a T-section constant – K high pass filter having cut-off frequency of 12 kHz and nominal impedance R_0= 500 Ω. Also find: (i) Its characteristic impedance and phase constant at 24 kHz and (ii) attenuation at 4 kHz.

4 What is an attenuator? Explain T-type attenuator and bridged T-type attenuator by deriving necessary equations.

5 (a) Explain the type of series generator with neat circuit diagram.

(b) The armature of a 2 – pole, 220 V Lap wound generator has 400 conductors and runs at 300 rpm. Calculate the useful flux / pole if the number of turns in each field coil is 1200.

6 A 50 kW, 440 V, shunt generator having an armature circuit resistance including the inter pole winding of 0.15 Ω at normal working temperature was run as a shunt motor on no load at its rated voltage and speed. The total current drawn by the motor was 5 A, including shunt field current of 1.5 A. Calculate the efficiency of shunt generator at full load.

7 A single phase transformer working at unity power factor has an efficiency of 90% at both half load, at full load of 600 W. Determine the efficiency at 80% of full load

8 Explain the principle of operation and characteristics of AC tacho meters.

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Code: 9A02401

2

II B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2012

PRINCIPLES OF ELECTRICAL ENGINEERING

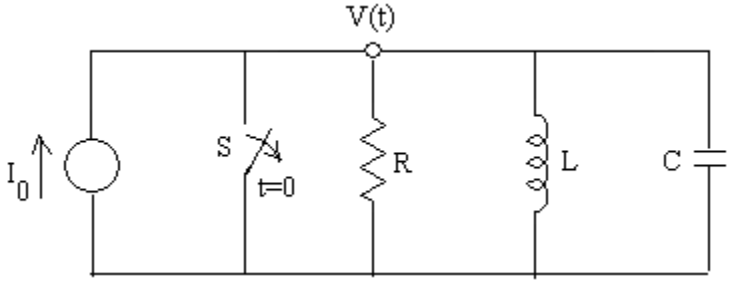
(Common to EIE, E. Con. E, ECE & ECC)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) Derive the expression for current when a dc voltage V is applied suddenly (i.e. at time = 0) by closing a switch in a series R-L circuit by using Laplace transform.

(b) Assuming zero initial conditions, Find V (t) given I_0=2 A, L=0.5 H, C=1F and R=0.5 Ω in the network shown in the fig below.



2 a) Define and obtain 'Y' - parameters by taking any one example.

b) A two port network has the following parameters: Z_{11}=20 Ω, Z_{12}=5 Ω, Z_{21}=20 Ω and Z_{22}=15 Ω. Calculate 'Y'- parameters.

3 Design an m-derived low pass filter to match a line having characteristic impedance of 600 Ω and to pass signals up to 500 Hz with infinite attenuation occurring at 750 Hz.

4 What is an attenuator? Explain T-type attenuator and Lattice attenuator by deriving necessary equations.

5 The armature of a 4-pole, lap wound shunt generator has 120 slots with 4 conductors per slot. The flux per pole is 0.05 Wb. The armature resistance is 0.05 ohm and the shunt field resistance 50 ohm. Find the speed of the machine when supplying 450 A at a terminal voltage of 250 V.

6 Explain the speed control of DC shunt motor by:
(i) Armature voltage control. (ii) Field flux control.

7 Explain the constructional details of a single phase transformer.

8 Explain the principle of operation and characteristics of AC servo motors.

*****

Code: 9A02401

3

II B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2012

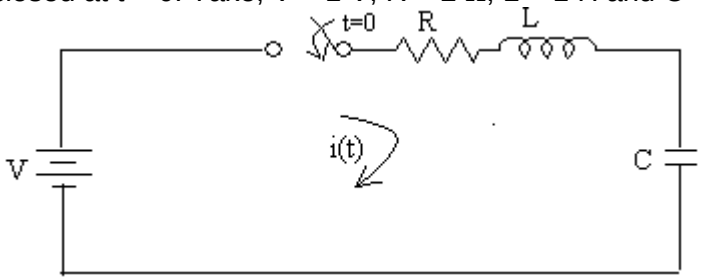
PRINCIPLES OF ELECTRICAL ENGINEERING

(Common to EIE, E. Con. E, ECE & ECC)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 For the network shown in the fig below, determine the expression for i (t). The switch is closed at t = 0. Take, V = 1 V, R = 2 Ω, L = 1 H and C = 0.5 F



2 (a) Define and obtain short circuit parameters by taking any one example.
(b) A two port network has the following parameters: Z_{11}=20 Ω, Z_{12}=5 Ω, Z_{21}=20 Ω and Z_{22}=15 Ω. Calculate admittance parameters.

3 Design an m-derived high pass filter having a design impedance of 600 Ω, cut-off frequency of 5 kHz and m=0.35. Also determine the frequency of infinite attenuation.

4 a) What is an attenuator? Derive the design equations for T-type attenuator.
b) Design a T-pad attenuator to give an attenuation of 60 dB and to work in a line of 500 Ω.

5 The armature of a 4-pole, wave wound shunt generator has 120 slots with 4 conductors per slot. The flux per pole is 0.05 Wb. The armature resistance is 0.05 ohm and the shunt field resistance 50 ohm. Find the speed of the machine when supplying 450 A at a terminal voltage of 220 V.

6 State the various methods to control the speed of a DC shunt motor and explain with neat circuit diagrams.

7 Explain the principle of operation of single phase transformer under no load and load conditions with neat phasor diagrams.

8 Explain the principle of operation and characteristics of capacitor motors.

*****

Code: 9A02401

4

II B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2012

PRINCIPLES OF ELECTRICAL ENGINEERING

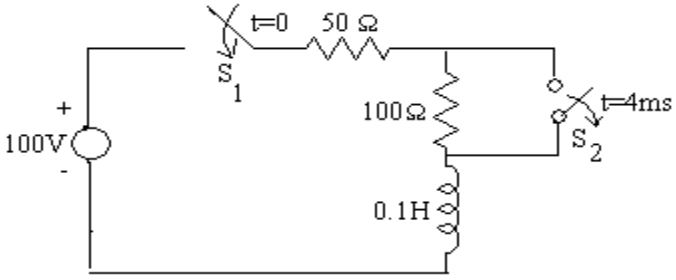
(Common to EIE, E. Con. E, ECE & ECC)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) Define and Short circuit admittance parameters by taking any one example.
(b) A two port network has the following parameters: Z_{11}=20 Ω, Z_{12}=5 Ω, Z_{21}=20 Ω and Z_{22}=15 Ω. Calculate ABCD parameters.

2 The circuit shown in fig below, the switch S_1 is closed at t=0 and switch S_2 is opened at t=4ms. Obtain 'i' for t>0 and sketch it.



3 Design a constant K –low pass filter having cut-off frequency 2.5 kHz and design resistance R_0=700 Ω. Also find the frequency at which this filter produces attenuation of 19.1 dB. Find its characteristic impedances and phase constant at pass band and stop or attenuation band.

4 a) What is an attenuator? Derive the design equations for π-type attenuator.
b) Design a T-pad attenuator to give an attenuation of 60 dB and to work in a line of 600 Ω.

5 A long-shunt compound generator supplies a load at 200 V through a pair of feeders of total resistance 0.04 ohm. The load consists of four motors, each taking 50 A and a lighting load of 100 bulbs each of 50 W. The armature resistance is 0.03 ohm, series field resistance 0.04 ohm and shunt field resistance 40 ohm. Find (i) Load current (ii) Terminal voltage and (iii) emf generated.

6 Explain the characteristics of DC motor.

7 Discuss the importance of open-circuit and short-circuit tests on a transformer, and also explain the procedure for open circuit and short circuit tests with neat circuit diagrams.

8 Explain the principle of operation and characteristics of shaded pole motors.

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