Code: 9A02503

III B. Tech I Semester (R09) Regular & Supplementary Examinations, November 2012

CONTROL SYSTEMS

(Common to EEE, E.Con.E, EIE, ECE & MCT)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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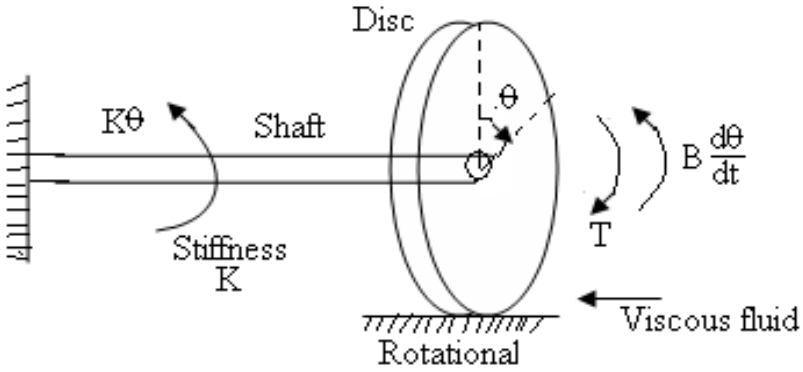
1 Derive the transfer function for the following rotational mechanical systems shown in the figure.



2 Derive the transfer function for a.c. servomotor. Explain about torque-speed characteristics of AC servomotor.

3 For a unity feedback control system the open loop transfer function
$G(s) = 10(s+2)/ s^2(s+1)$.Find: (a) position, velocity and acceleration error constants.
(b)Steady state error when the input $R(s) = (3/s)-(2/ s^2)+(1/3 s^3)$.

4 Sketch the root locus for the given system with $G(s)H(s)=(K(s+1))/(s (s+2))$.

5 (a) Define the following terms:
(i) Resonant peak (ii) Resonant frequency (iii)Band width (iv) Cut off rate

(b) Draw the Bode phase plot for the system having the following transfer function (s)=2000(s+1)/[s(s+10)(s+40)].

6 Check stability of the system by Nyquist criterion $G(s) = 10/[s^2(1+0.2s)(1+0.5s)]$.

7 Consider a unity feedback system with G(s) =75/(s+1) (s+3) (s+8). Design a PID controller to satisfy the following specifications.
(i) $K_v \geq 12$ (ii) Damping ratio = 0.6 (iii) ω_n = 2 rad/sec

8 A linear time invariant system is characterized by the state equation:

$$\begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} r(t)$$

With the step input and the initial conditions are $X_0 = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$.

Find the solution of the state equation.

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Code: 9A02503

III B. Tech I Semester (R09) Regular & Supplementary Examinations, November 2012

CONTROL SYSTEMS

(Common to EEE, E.Con.E, EIE, ECE & MCT)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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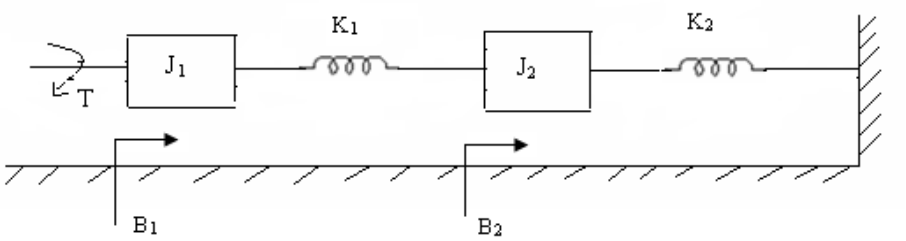
1 (a) Explain the following terms with respect to closed loop control systems:
(i) Plant (ii) Reference input (iii) Error detector (iv) Controller

(b) Write the differential equations governing the mechanical rotational systems shown in figure.



2 (a) Derive the transfer functions of an AC servomotor.

(b) Explain the operation and working principle of Synchro.

3 Consider a unity feedback system with a closed loop transfer function $\frac{C(s)}{R(s)} = \frac{Ks+b}{s^2+as+b}$. Determine the open loop transfer function G(s). Show that the steady state error with unit ramp input is given by (a-K)/b.

4 Consider the sixth-order system with characteristic equation
$s^6 + 2s^5 + 8s^4 + 12s^3 + 20s^2 + 16s + 16 = 0$. Comment on the stability.

5 Define the following terms: (i) Resonant peak (ii) Resonant frequency
(iii)Band width (iv) Cut off rate (v) Gain Margin (vi) Phase margin
(vii) Phase cross over frequency (viii)Gain cross over frequency

6 (a) Explain Nyquist stability criterion.

(b) In addition to providing absolute stability, the Nyquist criterion also gives information on the relative stability. Justify.

7 A unity feedback system has an open loop transfer function as G(s)=50/(s+3)(s+1). Design a PI controller so that phase margin of the system is 35^0 at a frequency of 1.2 rad/sec.

8 (a) Derive the expression for the transfer function from the state model.
$\dot{x} = Ax + Bu$ and $y = Cx + Du$

(b) Obtain state variable representation of an armature controlled D.C. motor.

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Code: 9A02503

3

III B. Tech I Semester (R09) Regular & Supplementary Examinations, November 2012

CONTROL SYSTEMS

(Common to EEE, E.Con.E, EIE, ECE & MCT)

Time: 3 hours Max. Marks: 70

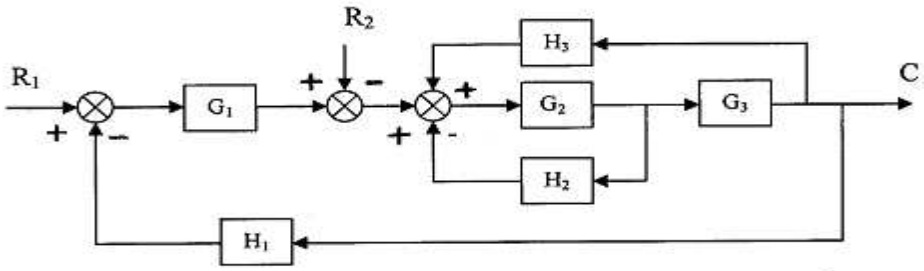
Answer any FIVE questions

All questions carry equal marks

*****

1 Distinguish between: (a)Linear and nonlinear systems
(b)Single variable and multi variable control systems
(c)Time – variant and time-invariant control systems
(d) Lumped and distributed control systems
Give an example for each of the above.

2 For the system represented in the given figure, obtain transfer function:
(a) C/R1 (b) C/R2



3 (a) Explain about various test signals used in the control systems.
(b) For the servomechanism with open loop transfer function given below, what type of input signal give rise to a constant steady state error and calculate their values
$G(s) = 10/ [s^2(s+1) (s+2)]$.

4 Sketch the root locus for the unity feedback system whose open loop transfer function is
$G(s) H(s) = K(s+1.5)/[s(s+1)(s+5)]$.

5 (a) Explain the procedure to determine the transfer function from bode plots.
(b) Draw the bode phase plot for the system having the following transfer function
$G(s)= 20/[s(1+3s)(1+4s)]$.

6 (a) How is Nyquist contour selected when the open loop transfer function has a pole at origin? Explain.
(b) Draw the polar plots for the following:
(a) $G(s) = 1/(1+sT)$ (b)$G(s) = 1/[s^2(1+sT_1)(1+sT_2)(1+sT_3)]$.

7 Consider a unity feedback system with open loop transfer function, $G(s)=20/s(s+2)(S+4)$. Design a PD controller so that the damping ratio of 0.8 and natural frequency of oscillations as 2 rad/sec.

8 Obtain the stat variable model in phase variable form for the following system:

$$\dddot{y} + 2\ddot{y} + 3\dot{y} + 4y = u(t).$$

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Code: 9A02503

4

III B. Tech I Semester (R09) Regular & Supplementary Examinations, November 2012

CONTROL SYSTEMS

(Common to EEE, E.Con.E, EIE, ECE & MCT)

Time: 3 hours Max. Marks: 70

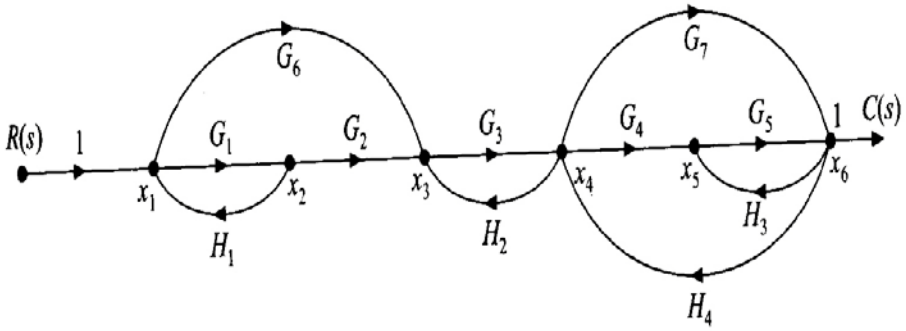
Answer any FIVE questions

All questions carry equal marks

*****

1 Define and explain the following terms:
(i) Characteristic equation.
(ii) Order of a transfer function.
(iii) Type of a transfer function.
(iv) Poles and zeros of a transfer function.

2 Obtain the transfer function using mason gain formula for the signal flow graph shown in figure.



3 (a) Define the following terms:
(i) Steady state error. (ii) Settling time.
(iii) Peak over shoot. (iv) Type and order of the control system.
(b) Find the steady state error for unit step, unit ramp and unit parabolic inputs for the following system: G(s) = 1000(s+1)/[(s+10)(s+50)]

4 Sketch the root locus for the unity feedback system whose open loop transfer function is $G(s)H(s)=K(s^2+6s+25)/[s(s+1)(s+2)]$.

5 Sketch the Bode plot for the transfer function given by G(s) H(s) = 2/[s(s+1) (1+0.2s)]. Also obtain gain and phase margin and cross over frequencies.

6 Sketch the polar plot for following transfer function and from the plot determine the phase margin and gain margin $G(s) = 200(s+2)/s(s^2 + 10s+100)$

7 Consider a unity feedback system with open loop transfer function, G(s)=K/s(2s+1)(0.5s+1). Design a suitable lag-lead compensator to meet the following specifications. (i) $K_v=30$ (ii) Phase margin ≥ 50.

8 (a) Define the terms (i) State variables and (ii) State transition matrix.
(b) Obtain the state model for a simple RLC series circuit.

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Code: 9A04501

III B. Tech I Semester (R09) Regular & Supplementary Examinations, November 2012

ANALOG COMMUNICATIONS

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) With the help of block diagram explain the elements of communication system.
(b) Explain how modulation can be used for efficient transmission.

2 (a) What are the practical considerations band pass systems? How practical carrier frequency and bandwidths are chosen?
(b) A certain transmitter radiates 6 KW with carrier unmodulated, and 9 kW when the carrier is sinusoid ally modulated. Calculate the modulation index. If another sine wave is simultaneously transmitted with modulation index of 0.5, determine the total radiated power.

3 (a) What are the advantages and disadvantages of generating AMSSB using filter method?
(b) A 500 W carrier is amplitude modulated to a depth of 75%. Calculate the total power in case of SSB technique. How much power saving is achieved for SSB compared to AM and DSBSC?

4 (a) Explain how FM can be generated from PM.
(b) What is the need for amplitude limiter circuit in FM?

5 (a) What are the limitations of slope detector?
(b) The mutual conductance of an FET varies linearly with gate voltage between the limits of 0 to 9 mS. The FET is used as a capacitive reactance modulator, with X_{Cgd} = 10 Rgs and is placed across an oscillator circuit which is tuned to 50 MHz by a 50 pF fixed capacitor. What will be the total frequency variation when the trans conductance of the FET is varied from zero to maximum by the modulating voltage?

6 Draw the block diagram Super Heterodyne Receiver and functionality of each block.

7 Discuss about noise effect in AM and obtain expression for figure of merit. Consider large noise case.

8 With neat wave forms explain about:
(i) Natural PAM sampling.
(ii) Flat-top PAM sampling.

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Code: 9A04501

2

III B. Tech I Semester (R09) Regular & Supplementary Examinations, November 2012

ANALOG COMMUNICATIONS

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Discuss about different modulation methods.
(b) Explain the benefits of coding.

2 (a) Draw and explain the band pass signal and spectrum.
(b) The antenna current of an AM transmitter is 9 A when only the carrier is sent, but it increases to 10.6 A when the carrier is modulated by a single sine wave. Find the percentage modulation. Determine the antenna current when the percentage of modulation changes to 0.8.

3 (a) Compare the different AM systems.
(b) Discuss the frequency translation techniques using square wave carrier.

4 (a) Compare the narrow band FM and AM.
(b) What is the need for amplitude limiter circuit in FM.

5 (a) With the help of block diagram, explain about narrow band phase modulator.
(b) The mutual conductance of an FET varies linearly with gate voltage between the limits of 0 to 9 mS. The FET is used as a capacitive reactance modulator, with X_{Cgd} = 6 Rgs and is placed across an oscillator circuit which is tuned to 40 MHz by a 40 pF fixed capacitor. What will be the total frequency variation when the trans conductance of the FET is varied from zero to maximum by the modulating voltage?

6 (a) Draw and explain typical selectivity curve of radio receiver.
(b) Discuss about choice of IF in Super Hetero Dyne receiver.

7 Discuss about noise effect in AM and obtain expression for figure of merit. Consider small noise case.

8 With help of the circuits, explain about PAM modulator and de-modulator.

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3

Code: 9A04501

III B. Tech I Semester (R09) Regular & Supplementary Examinations, November 2012

ANALOG COMMUNICATIONS

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) What are the benefits of modulation? Explain in detail.
(b) Explain different coding methods used in communication.

2 (a) Derive an expression for modulation index of multi tone AM signal.
(b) Explain about a switching modulator. Draw the necessary circuit and waveform.

3 (a) Sketch the spectrum of suppressed carrier AM systems. Assume Sinusoidal carrier and sinusoidal modulating signal.
(b) Discuss the effects of frequency errors in synchronous detection of AMDSB – SC.

4 (a) Derive the expression band width of FM.
(b) In an FM system, when an audio frequency is 500 Hz, and the AF voltage is 2.4 V, the frequency deviation is 4.8 KHz. If the AF voltage increased to 10 V while audio frequency dropped to 300 Hz, then what is the new deviation. Find the modulation index in each case.

5 With the help of block diagram and relevant waveforms, explain the operation of switching circuit modulator.

6 (a) Define Image frequency in a receiver and explain what is the need for its rejection.
(b) Discuss about choice of IF in Super Hetero Dyne receiver.

7 Discuss about noise effect in AMSSB-SC and obtain expression for figure of merit.

8 With necessary block diagrams explain about PWM system.

*****

4

Code: 9A04501

III B. Tech I Semester (R09) Regular & Supplementary Examinations, November 2012

ANALOG COMMUNICATIONS

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) What are the applications of modulation? Explain in detail.
(b) What are the applications of coding methods? Explain in detail.

2 (a) Describe the generation of AM signals using non linear devices.
(b) Considering modulating signal as a square wave that switches periodically between + 2 and -2.Sketch amplitude modulated signal with carrier and suppressing carrier. Assume the modulation index is 0.5.Indicate the envelopes by dashed lines.

3 (a) Discuss the benefits of suppressed carrier AM systems.
(b) Describe the generation AMSSB using phase shift method.

4 (a) What is the bandwidth required for FM signal, give the necessary reasons.
(b) Obtain and sketch the phasor diagram of single tone NBFM.

5 (a) Explain the generation FM using direct method.
(b) Compare slope detector and balanced slope detector.

6 (a) Discuss about separately Excited Mixer.
(b) In a broadcast Super Heterodyne Receiver having no RF amplifier, the loaded Q of the antenna coupling circuit is 100. If the Intermediate frequency is 455 kHz, calculate:
(i) The image frequency and its rejection ratio at 1 MHz (ii) The image frequency and its rejection ratio at 25 MHz.

7 (a) Explain about threshold effect in FM.
(b) Two resistors of 20 K Ohms and 50 K Ohms, are at room temperature. Calculate for a bandwidth of 100 kHz, the thermal noise voltage (i) For each resistor (ii) When two resistors are in series (iii) When two resistors are in parallel. Assume $kT = 4 \times 10^{-21}$ W/Hz at room temperature.

8 With the help of waveform illustrations explain different type's pulse modulation systems.

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Code: 9A04502

1

B.Tech III Year I Semester (R09) Regular and Supplementary Examinations, November 2012

LINEAR IC APPLICATIONS

(Electronics and Communication Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) List and compare the different configurations of differential amplifier.

(b) Calculate the amplification factor for AC signal input in dual input balanced output differential amplifier.

2 (a) Draw and Explain the block diagram of Op-Amp.

(b) Explain the term “Slew Rate” and how it affects the frequency response of an OP-AMP wit suitable examples?

3 (a) Draw a neat circuit diagram of an AC inverting amplifier. What are the major advantages and disadvantages of a single supply AC amplifier?

(b) In an AC inverting amplifier circuit R_{in} = 50 Ω, C_i = 0.1μF, R_1 = 100 KΩ, R_f = 1KΩ, R_2 = 10 KΩ and V_{CC} = ±15V. Determine the bandwidth of the amplifier

4 (a) What is the difference between a basic comparator and the Schmitt trigger? Construct a Schmitt trigger circuit using OP-AMP and derive the threshold voltages.

(b) Explain the operation of a free running astable multivibrator used as square wave generator.

5 (a) A Particular application requires that all frequency below 400 Hz should attenuate. The attenuation should be at least -22 dB at 100 Hz. Design a filter to meet this requirement.

(b) What do the characteristics of order and poles indicate.

6 (a) Explain the operation of astable multivibrator using 555 timers.

(b) Design a square waveform generator of frequency 1 kHz and duty cycle of 75%using 555 timers.

7 (a) What are the basic blocks preceding an Analog to Digital converter in a typical application like digital audio recording?

(b) With the help of a neat circuit diagram and waveforms, explain the operation of a dual slope ADC. What are its special features?

8 What are all basic blocks of analog multiplexer? Explain how the data selections process is performed it.

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Code: 9A04502

2

B.Tech III Year I Semester (R09) Regular and Supplementary Examinations, November 2012

LINEAR IC APPLICATIONS

(Electronics and Communication Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions

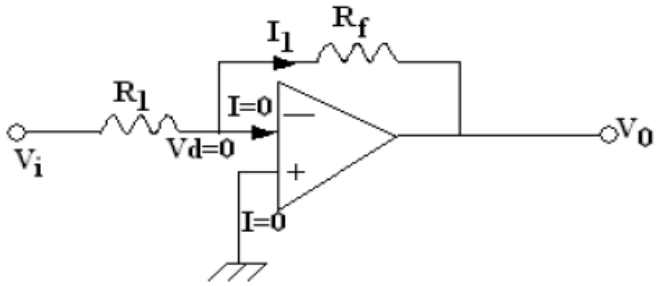
All questions carry equal marks

*****

1 (a) Draw the schematic of emitter coupled differential amplifier, explain the operation.

(b) What is level translator? What is the necessity of level translator stage in cascading of differential amplifiers?

2 (a) Calculate the exact closed loop gain of inverting amplifier shown in figure if AOL = 200 KΩ, Ri = 2 MΩ and R0 = 75Ω.



(b) What are the three differential amplifier configurations? Compare and contrast these configurations.

3 (a) Derive the output voltage of an Op-Amp based differential amplifier.

(b) Draw the circuit of a typical instrumentation amplifier. Why do we use two stage op-Amp circuits as an instrumentation amplifier? Explain

4 (a) Draw the circuit diagram and sketch the input, output waveforms of an astable multivibrator using op-amp.

(b) Derive the expressions for T1 and T2 of an astable multivibrator.

5 (a) Define pass band and stop band of filter.

(b) Design a band pass filter so that f_0 = 2KHz,Q = 20 and A_0 = 10 Choose c = 1μF

6 (a) Draw the circuit of PLL as frequency multiplier and explain its working.

(b) Explain block schematic of PLL. List the application of PLL.

7 (a) Explain the operation of a dual slope type Analog to Digital converter.

(b) A dual slope Analog to Digital converter uses a 16-bit counter and operates at 4 MHz clock rate. The maximum input voltage is + 8volts. Find the value of integrator resistor 'R' if the maximum output voltage of the integrator is - 6 volts after 2n counts for an integrator capacitor of 0.1μF.

8 Explain the use IC 1496 as AM modulator with necessary circuit diagram.

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Code: 9A04502

3

B.Tech III Year I Semester (R09) Regular and Supplementary Examinations, November 2012

LINEAR IC APPLICATIONS

(Electronics and Communication Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions

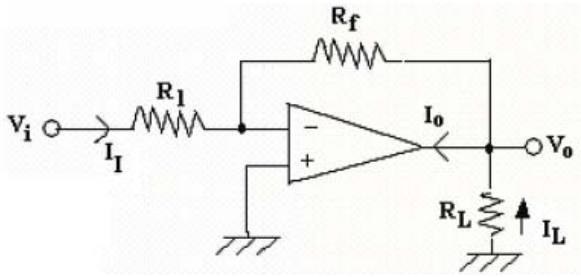
All questions carry equal marks

*****

1 (a) Draw the transfer characteristics of differential amplifier. Mention the advantages and limitations.
(b) Draw the equivalent circuit of emitter coupled differential amplifier from which calculate A_C.

2 (a) Explain the procedure for measuring offset voltage and bias currents of general purpose Op-Amp.
(b) With neat block diagram explain the function of various building blocks of an OP-AMP.

3 (a) Draw the circuit diagram of inverting amplifier and explain the operation.
(b) For the circuit shown in figure below calculate I_1, I_L and V_O with R_1 = 10 KΩ, R_f =100 KΩ, Vi = 1V, R_L = 25 KΩ.



4 (a) With suitable circuit diagram explain the operation of a triangular wave generator using a comparator and a integrator.
(b) Draw a sample and hold circuit and explain its operation with necessary input and output waveforms and indicate its uses.

5 (a) What are the two conditions to have satisfactory operation of wide band reject filter?
(b) Design a wide band reject filter having F_H = 400 Hz and F_L = 2 KHz with a pass band gain of 2.

6 (a) Draw the block schematic of a 566 voltage controlled oscillator IC.
(b) Derive an expression for the voltage to frequency conversion factor of 566 VCO.

7 (a) Explain the operation of a counter type of Analog to Digital converter.
(b) Specify the modifications necessary in the circuit for a time varying analog input voltage.
(c) Calculate the conversion time for a full scale input in case of a 12-bit counter type Analog to Digital converter driven by 2 MHz clock.

8 Derive the output voltage expression for:
(a) Frequency doublers.
(b) Phase angle detection.

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Code: 9A04502

4

B.Tech III Year I Semester (R09) Regular and Supplementary Examinations, November 2012

LINEAR IC APPLICATIONS

(Electronics and Communication Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) List out different configurations of differential amplifier. Explain any one of them in detail.
(b) Explain the use of constant bias circuit in operation of differential amplifier.

2 (a) Draw the internal block diagram of an operation amplifier. Explain the operation of each block.
(b) Define Drift. Explain how drift can be compensated in Op-Amps with proper example.

3 (a) Explain how the operational amplifier can be used as a Differentiator and Integrator.
(b) What is a voltage follower? What are its features and applications?

4 (a) Distinguish between astable, bistable and monostable multivibrators.
(b) With the help of a neat circuit diagram explain the working of a logarithmic amplifier.

5 (a) Design a Twin –T notch filter?
(b) Draw & explain the frequency response of Twin-T notch filter.

6 (a) Draw the schematic circuit diagram of the following and explain their working.
(i) Analog phase detector
(ii) VCO. Derive necessary expressions.
(b) What is their role is in PLL? Explain.

7 (a) With a neat circuit diagram explain the functioning of an inverted R-2R ladder type Digital to Analog converter
(b) The LSB of a 10-bit DAC is 20 m volts.
(i) What is its percentage resolution?
(ii) What is its full-scale range?
(iii) What is the output voltage for an input, 10110 01101?

8 (a) Draw the circuit diagram of sample and hold circuit and explain its working.
(b) Draw the circuit diagram IC 1496 balanced modulator circuit and explain its Operations. Sketch the output waveform for the square wave inputs with a Phase difference ‘φ’.

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1

Code: 9A04503

B.Tech III Year I Semester (R09) Regular & Supplementary Examinations, November 2012

ANTENNAS AND WAVE PROPAGATION

(Electronics and Communication Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Explain the following:
(i) Antenna gain. (ii) Antenna temperature. (iii) Retorted potential

(b) Evaluate the directivity of an isotropic source and source with bidirectional 'coso' power pattern.

2 (a) Derive expression for an oscillating current element and prove that the radiations resistance $R_r = 80\ \lambda^2\left(\frac{dl}{\lambda}\right)^2\ \Omega$.

(b) Explain about radiation power and effective height.

3 (a) Show that the directivity of a broad side array L>>d is $D_0 = 2\ (\frac{d}{\lambda})$.

(b) Explain pattern multiplication with appropriate examples.

4 (a) How horn antenna can be constructed and explain different horn antennas.

(b) Explain about construction and operation of yagi-ude antenna.

5 (a) Explain about micro strip antennas with neat diagrams.

(b) What is a parabolic cylinder antenna? Derive an expression for field distributions on the surface of the reflector.

6 (a) Explain about zoned lens antennas.

(b) Describe the method for measuring the gain and radiation pattern of an antenna.

7 (a) Explain about ground wave propagation with its characteristics.

(b) Explain in detail about duct propagation and what are its advantages over other propagation.

8 (a) Draw the structure of ionosphere and how it varies with weather explain in detail.

(b) Explain the following:
(i) Virtual height. (ii) Skip distance. (iii) Multi-hap propagation.

*****

2

Code: 9A04503

B.Tech III Year I Semester (R09) Regular & Supplementary Examinations, November 2012

ANTENNAS AND WAVE PROPAGATION

(Electronics and Communication Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Explain the following:
(i) Antenna field zones. (ii) Effective height. (iii) Effective operative.
(b) Determine the effective operative and directivity of a linear λ/2 dipole antenna.

2 (a) Prove that the radiation resistance of a current element is $R_r = 80 \lambda^2 (\frac{dl}{\lambda})^2 \Omega$.
(b) Write about effective area and beam width.

3 (a) Differentiate linear and binomial arrays.
(b) Give the mathematical relations for an 'N' elements spaced by λ/2 wave length. If N = 20 find the HPBW and directivity.

4 (a) What is V-antenna and explain its characteristics.
(b) Explain about and travelling wave antenna with neat diagram and necessary expressions.

5 (a) Directivity of an horn antenna can be measured. Explain in details.
(b) What are the different parameters effects the characteristics of micro strip antennas explain?

6 (a) Explain about non-metallic dielectric antennas in detail.
(b) What is the principle of equality of path length? How it is applicable to horn antenna.

7 (a) What are the different mechanisms of EM wave's propagation? Explain.
(b) Derive a relation for MUF.

8 (a) Explain about super refraction, with neat diagrams.
(b) Derive a relation for virtual height and skip distance.

*****

Code: 9A04503

3

B.Tech III Year I Semester (R09) Regular & Supplementary Examinations, November 2012

ANTENNAS AND WAVE PROPAGATION

(Electronics and Communication Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 Explain and find the effective length of a λ/2 dipole and λ/4 monopole and calculate their directivities using the appropriate radiation resistance.

2 (a) State and prove reciprocity theorem for antenna.
(b) Explain about linear wire antennas with neat diagrams.

3 (a) What is the need of antenna arrays? Explain three different types of arrays.
(b) A uniform linear array consists of 16 isotropic point source with a spacing of λ/4.
Find (i) HPBW. (ii) Directivity. (iii) Effective aperture, assume required phase difference.

4 (a) A Rhombic antenna can be constructed using V- antenna and inverted V-antenna, explain.
(b) Explain about travelling wave antenna.

5 (a) Explain about different feed methods for an antenna with neat diagram.
(b) Explain about flare sheet, corner and paraboloidal reflectors.

6 (a) Explain different tolerances an lens antenna with relevant expressions.
(b) A standard gain horn antenna with power gain of 12.5 is used to measure the gain of a large directional antenna by comparison method. The test antenna is connected to the receiver and all attenuation adjusted to 23 dB in order to have the same receiver output. Find the gain of the large antenna.

7 (a) Explain about ground wave propagation in detail with neat diagrams and examples.
(b) Explain about effect of earth curvature with relevant expressions.

8 (a) Draw the structure of ionosphere and how waves propagate though it, explain in detail.
(b) Explain the following:
(i) Skin depth. (ii) Virtual height. (iii) Energy loss in ionosphere.

*****

4

Code: 9A04503

B.Tech III Year I Semester (R09) Regular & Supplementary Examinations, November 2012

ANTENNAS AND WAVE PROPAGATION

(Electronics and Communication Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Explain the following:
(i) Antenna radiation pattern. (ii) Radiation intensity. (iii) Beam efficiency.
(b) Determine the directivity of the following source.
(i) $u = u_m \cos^3\theta$. (ii) $u = u_m \sin\theta \sin^2\theta$.

2 (a) Determine an expression for radiation resistance for a monopole antenna.
(b) What are the applications of loop antenna?

3 (a) Explain array of two point sources.
(b) What is antenna array, explain different array antennas.

4 (a) Explain the helical antenna structure and characteristics with neat diagram.
(b) Explain about pyramidal horn antennas in detail.

5 (a) Explain about micro strip antennas and give its limitations and advantages.
(b) Discuss the application of the image antenna concept to the 90^0 corner reflector.

6 (a) Explain about H-plane metal plate lens antennas with neat diagrams and explain.
(b) Write short notes on radiation from “Sectoral Horn”

7 (a) What are different mechanisms of propagation of electromagnetic waves? Explain in detail.
(b) Explain about scattering phenomina and super refraction.

8 (a) Derive relation between MUF and skip distance.
(b) Explain about energy loss in ionosphere and reflection of sky wave by ionosphere in detail.

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Code: 9A04504

1

III B. Tech I Semester (R09) Regular & Supplementary Examinations, November 2012

DIGITAL IC APPLICATIONS

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Draw the logic diagram equivalent to the internal structure of an 8-input CMOS NAND gate.
(b) Show the transistor circuit for this gate and explain the operation with the help of function table.

2 (a) Draw the circuit diagram of basic CMOS gate and explain its operation.
(b) What are the typical parts of a TTL data sheet and discuss their importance in circuit design?

3 (a) Design a logic circuit to detect prime number of a 4-bit input. Write the VHDL program for the above design.
(b) Design the logic circuit and write a data-flow style VHDL program for the following function. $F(P) = \sum_{A,B,C,D} (1,5,6,7,9,13) + d(4,15)$.

4 (a) With the help of logic diagram explain 74×157 multiplexer.
(b) Write the data flow style VHDL program for this IC.

5 Draw the structure of a 4-bit comparator and briefly explain about it. Write a structural VHDL code for it.

6 Write a VHDL code for 8 bit comparator circuit. Using this entity write a VHDL code for 24 bit comparator. Use the structural model for it.

7 (a) Distinguish between the ring counter and ripple counters.
(b) Design a mod-129 counter using only two 74X163s and no additional gates.

8 Draw the block diagram of SRAM with a bidirectional data bus. Explain its operation.

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Code: 9A04504

2

III B. Tech I Semester (R09) Regular & Supplementary Examinations, November 2012

DIGITAL IC APPLICATIONS

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Design a 4-input CMOS AND-OR-INVERT gate. Draw the logic diagram and function table.

(b) Draw the resistive model of a CMOS inverter and explain its behavior for LOW and HIGH outputs.

2 (a) Explain the difference in program structure of VHDL and any other procedural language. Give an example.

(b) Explain sinking current and sourcing current of TTL output. Which of the above parameters decide the fan-out and how?

3 (a) Write a VHDL entity and Architecture for the following function.

$F(x) = (a + b)\ (c \oplus d)$

Also draw the relevant logic diagram.

(b) Write a VHDL entity and architecture for a 3-bit ripple counter using Flip-Flops.

4 Design the logic circuit and write a data-flow style VHDL program for the following functions:

(a) $F(X) = \sum_{A,B,C,D} (0, 2, 5, 7, 8, 10, 13, 15) + d (1, 6, 11)$.

(b) $F(Y) = \prod_{A,B,C,D} (1, 4, 5, 7, 9, 11, 12, 13, 15)$.

5 Draw the logic diagram, logic symbol of 74x245 octal 3- state trans-receiver and explain its operation.

6 Design a floating point encoder with 74x151 and 74X148 ICs and its VHDL code.

7 Show the logic diagram of 74X175 IC and write VHDL code for it in data flow model. Using this entity, develop the program for 16 bit register and show the corresponding circuit and also explain how the register is cleared.

8 Write short notes on:

(a) RAM (b) SSRAM (c) DRAM (d) SDRAM.

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Code: 9A04504

3

III B. Tech I Semester (R09) Regular & Supplementary Examinations, November 2012

DIGITAL IC APPLICATIONS

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Design CMOS transistor circuit for 3-input AND gate. With the help of function table explain the circuit.

(b) Draw the CMOS circuit diagram of tri-state buffer. Explain the circuit with the help of logic diagram and function table.

2 (a) Draw the circuit diagram of basic CMS gate and explain the operation.

(b) List out different categories of characteristics in a TTL data sheet. Discuss electrical and switching characteristics of 74 LS00.

3 Design the logic circuit and write a data-flow style VHDL program for the following functions:

(a) $F(P) = \Pi_{A,B,C,D}(1,7,9,13,15)$.

(b) $F(Y) = \sum_{A,B,C,D}(1,4,5,7,12,14,15) + d(3,11)$.

4 (a) Write a VHDL program for 74×245.

(b) Design a 16-bit comparator using 74×85 Ics.

5 Write a data flow VHDL code for a 7 segment display indicating 0, 1, 2.

6 What is a comparator? Explain the operation of a 2-bit comparator with a relevant diagram. Draw its logic symbol and write a VHDL code for it.

7 Design a modulo 16 counter, using one 74X169 with the following sequence 7,6,5,4,3,2,1,0,8,9,10,11,12,13,14,15,7….

8 Draw and explain the structure of an 8X4 static RAM.

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Code: 9A04504

4

III B. Tech I Semester (R09) Regular & Supplementary Examinations, November 2012

DIGITAL IC APPLICATIONS

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Design a three input NAND gate using diode logic and a transistor inverter. Analyze the circuit with the help of transfer characteristics.
(b) Explain how a CMOS device is destroyed.

2 (a) Draw the circuit diagram of basic CMS gate and explain the operation.
(b) Design a transistor circuit of 2-input ECL NOR gate. Explain the operation with the help of function table.

3 (a) Explain the various data types supported by VHDL. Give the necessary examples.
(b) Discuss the case statement and its use in VHDL program.

4 Design a 10 to 4 encoder with inputs 1- out of 10 code and outputs in BCD. Provide the data flow style VHDL program.

5 Draw a logic symbol for 8 sources sharing a 3 state priority line using a 74X138 decoder. And write a VHDL programme using a case statement.

6 Explain how EXOR and EXNOR gates will be used for comparing the data. And explain 4 bit magnitude comparator.

7 (a) Design an 8 bit synchronous binary counter with serial enable control.
(b) Write short notes on counter applications.

8 Write short notes on different ROMs and RAMs.

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Code: 9A05406

1

III B. Tech I Semester (R09) Regular & Supplementary Examinations, November 2012

COMPUTER ORGANIZATION

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Explain the basic performance equation.
(b) Explain the process of error detection using parity bit with an example.

2 (a) Explain the key design elements of most RISC systems.
(b) A computer has 32 bit instructions and 12 bit addresses. If there are 250 two-address instructions, how many one address instructions can be formulated.

3 (a) Draw the general block diagram of microprogram sequencer. Explain clearly the inputs and outputs of the same along with their functioning.
(b) Explain how the mapping from an instruction code to a micro instruction address can be done by means of a read only method. What is the advantage of this method?

4 (a) Explain the one stage decimal arithmetic unit.
(b) Explain the flow chart of decimal multiplication and decimal division operations.

5 (a) Describe the basic concepts of semiconductor RAM memories.
(b) Give short notes on cache memories.

6 (a) Distinguish between synchronous and asynchronous data transfer modes.
(b) Give short notes on interconnect bus.

7 Define pipelining. List out the types of pipelining. Explain in detail.

8 (a) Explain parallel arbitration logic.
(b) Discuss the data transfer abnormalities.

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Code: 9A05406

2

III B. Tech I Semester (R09) Regular & Supplementary Examinations, November 2012

COMPUTER ORGANIZATION

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Discuss in brief about multiprocessors and multicomputers.
(b) Explain the pipelining and superscalar operation.

2 (a) Design a single bus line with three state buffers.
(b) There exists three 4-bit registers (A, B and C) and 4-bit data lines (say D). Design a circuit to transfer data from any register to any other register including data lines and vice versa.

3 (a) What is microinstruction? Give the typical horizontal and vertical microinstruction formats and compare them.
(b) Discuss about the design considerations of microinstruction sequencing technique.

4 (a) Write short notes on array multiplier.
(b) Explain the operation of restoring division with flow chart.

5 Explain the need for memory Hierarchy and discuss the reasons for not having a large enough main memory for storing the total information in a computer system.

6 (a) Explain about input-output interface.
(b) Discuss about serial communication protocols.

7 How does conditional branch instruction affect the performance of instruction pipelining? Explain with the help of timing diagram.

8 (a) Explain interprocessor communication and synchronization.
(b) Write algorithm for generation of dynamic arbitrations.

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Code: 9A05406

3

III B. Tech I Semester (R09) Regular & Supplementary Examinations, November 2012

COMPUTER ORGANIZATION

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Differentiate traditional bus architecture from high performance bus architecture.
(b) Write a brief note on Hamming code.

2 (a) With a neat sketch explain the 4 bit combinational circuit shifter.
(b) Starting from an initial value of R = 11011101, determine the sequence of binary values in R after logical shift left, followed by a circular shift-right, followed by a logical shift-right and a circular shift-left.

3 (a) What is a pipe line register? What is the use of it? Explain in detail.
(b) Explain the variety of techniques available for sequencing of micro instructions based on the format of the address information in the micro instruction.

4 (a) Draw a flow chart for multiplication of floating point numbers and explain it.
(b) Explain the sign magnitude representation and 2's complement representation of a number. What are the advantages of 2's complement representation over sign magnitude representation?

5 Briefly explain the memory device characteristics that are considered while designing a memory system for a computer.

6 (a) Explain Asynchronous data transfer modes.
(b) Explain priority interrupt direct memory access.

7 (a) What is parallel processing? What is meant by instruction stream and data stream?
(b) How the synchronization problems can be solved by using a semaphore?

8 (a) Explain centralized shared memory architecture.
(b) Explain the write operations to be performed on cache memory.

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Code: 9A05406

4

III B. Tech I Semester (R09) Regular & Supplementary Examinations, November 2012

COMPUTER ORGANIZATION

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Explain the characteristics of multiprocessors.
(b) Compare machine language, assembly language and high level language.

2 (a) Differentiate between RISC and non-RISC systems.
(b) Design a circuit for parallel load operation into one of the four 4-bit registers from a bus. Mention clearly control/selection bits and selection logic. Assume JK flip flops.

3 (a) Formulate a mapping procedure that provides eight consecutive micro instructions for each routine. The operation code has six bits and the control memory has 2048 words.
(b) Draw and explain the block diagram of hardwired control unit.

4 (a) What is a Booth's algorithm for 2's complement multiplication? Explain with an example.
(b) How many bits are needed to store the result addition, subtraction, multiplication and division of two n-bit unsigned numbers?

5 (a) What is cache memory? Explain its operation.
(b) Brief out the hardware organization of associate memory.

6 (a) Explain about data transfer modes.
(b) List the salient features about standard serial communication protocols.

7 (a) Explain SIMD processor organization.
(b) Give the applications of array processors.

8 (a) Explain distributed shared memory architecture.
(b) Explain cache coherence.

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