Code: 9A02601

1

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

POWER SEMICONDUCTOR DRIVES

(Electrical & Electronics Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
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1 (a) Explain the constant power mode and constant torque modes of operation of separately excited d.c motor drives.

(b) A 220 V, 1200 rpm, 120 A separately excited DC motor is fed from 1-Φ, fully controlled converter with an ac source 230 V, 50 HZ supply. The thyristor is triggered continuously by a dc signal. The resistance of armature circuit is 0.07 Ω. Find the firing angle for rated motor torque and (-700) rpm.

2 Draw the power circuit diagram and explain the operation of three phase full converter drives and also explain the output voltage and current waveforms at firing angle of 60^0, 90^0, 120^0.

3 (a) Explain how four-quadrant operation is achieved by dual converters each of 3 φ full wave configuration for d.c. separately excited motor.

(b) Distinguish between circulating current and non-circulating current mode of operation.

4 Explain the operation of four quadrant chopper fed to the D.C series motor and also draw the current and voltage wave forms for continuous current operation.

5 (a) The power switches can be connected in a number of ways to the star and delta connected stator of an induction motor for speed control using stator voltage control. Enumerate the variations.

(b) Constant torque loads are not suitable for AC Voltage controller fed induction motor drive. Why?

6 Explain how PWM inverter eliminate the drawbacks of cyclo - converter fed Induction motor drives

7 (a) What is slip power recovery? What modifications can be suggested for improving the power factor of the slip energy recovery scheme?

(b) Explain the principle of operation of static Kramer drive.

8 Describe the converter used for low frequency high power synchronous motor drives with relevant wave forms.

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Code: 9A02601

2

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

POWER SEMICONDUCTOR DRIVES

(Electrical & Electronics Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
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1 (a) Explain how the speed of a dc series motor is controlled using converters.
(b) A dc series motor has Ra = 3 Ω, Rf = 3 Ω and Maf = 0.15 H. The motor speed is varied by a phase-controlled bridge. The firing angle is π /4 and the average speed of the motor is 1450 rpm. The applied ac voltage to the bridge is 330 Sin wt. Assuming continuous motor current find the steady state average motor current and torque. Sketch the waveforms for output voltage, current and gating signals.

2 Explain the speed torque characteristics of a dc series motor connected to a three-phase fully controlled converter.

3 (a) Explain the operation of four quadrant chopper fed to the D.C series motor and also draw the current and voltage waveforms for continuous current operation.
(b) A dc shunt motor has the armature resistance of 0.04 Ω and the field winding resistance of 10 Ω. Motor is coupled to an over hauling load with a torque of 400 N-m. Following magnetization curve was measured at 600 rpm:

Field current, A	2.5	5	7.5	10	12.5	15	17.5	20	22.5	25
Back emf, V	25	50	73.5	90	102.5	110	116	121	125	129

Calculate the value of R_B when the motor is required to hold overhauling load at 1200 rpm.

4 (a) Explain the dynamic breaking of D.C series motor by chopper control.
(b) A class-A chopper, operating in time-ratio control, is supplying the armature of the separately excited dc motor. Derive the motor speed-torque relationship.

5 A 3 phase, 6 pole, star connected squirrel cage induction motor is to be controlled by terminal voltage variation using pairs of inverse parallel connected thyristors on each supply line. Sketch a diagram of this arrangement and list the merits and demerits of thyristor control using symmetrical phase angle triggering. Also draw voltage and current wave forms.

6 Explain the working of closed loop CSI fed induction motor drive with a neat block diagram.

7 (a) Describe the operation of induction motor speed control using static rotor resistance variation.
(b) Derive the relation between rotor circuit resistance and duty ratio.

8 (a) Explain why cyclo - converter fed synchronous motors are preferred for low speed applications.
(b) Explain why frequency must be changed in small steps in true synchronous motor mode.

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Code: 9A02601

3

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

POWER SEMICONDUCTOR DRIVES

(Electrical & Electronics Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 Write the basic performance equations for a D.C series motor. Sketch characteristics of constant torque drive and constant power drive regions.

2 (a) A 220 V, 1200 rpm, 60 A separately excited DC motor with armature resistance of 0.6 ohm, is fed from 3-phase, fully controlled converter with an ac source line voltage 415 V, 50 Hz supply. A star connected transformer is used to feed the armature so that motor terminal voltage equals rated voltage when converter firing angle is zero. Calculate transformer turns ratio.

(b) Explain the speed-torque characteristic of 3-ohm fully controlled converter feeding DC series motors with relevant waveforms.

3 (a) What are the differences between the ideal and practical dual converters applied for the control of dc motors?

(b) If the motor is operated under dynamic breaking at twice the rated torque and 1000 rpm then calculate the value of breaking current and resistor by assuming linear magnetic circuit.

4 A 220 V, 200 A dc series motor has armature and field resistances of 0.03 and 0.02 Ω respectively. Running on no load as a generator with field wining connected to a separate source it gave following magnetization characteristic at 750 rpm.

Field current , A	40	80	120	160	200
Terminal Voltage, v	52	108	148	176	189

Motor is controlled by a chopper in dynamic braking with a braking resistance of 2 Ω.
(a) Calculate motor speed for a duty ratio of 0.7 and motor current of 150 A.
(b) What will be the motor speed for a duty ratio of 0.75 and motor torque equal to half of rated torque?

5 From the fundamentals derive the expression for torque and explain the speed torque characteristics of induction motor.

6 Compare the operation of cyclo-converter fed induction motor drives with PWM inverter fed Induction motor drives

7 Explain the operation of 3-phase Induction motor with chopper controlled resistance in the rotor circuit with a neat schematic. Mention the advantages and disadvantages of the above method of control.

8 (a) Explain the role of damper windings in synchronous motor.

(b) How the operation of a synchronous motor shifts from motoring to regenerative braking?

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Code: 9A02601

4

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

POWER SEMICONDUCTOR DRIVES

(Electrical & Electronics Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) Explain speed-torque characteristics of a 1- Φ fully controlled converter connected to separately excited D.C motor with continuous current operation. Draw the relevant wave forms.
(b) Explain the operation of single phase semi-converter fed separately excited d.c. Motor drive with necessary diagrams.

2 Explain the speed - torque characteristics of a separately excited dc motor connected to a three phase semi controlled converter.

3 (a) A single-phase fully controlled thyristor converter is supplying a separately excited DC motor. Draw the relevant waveforms and explain various operating modes of the drive both in motoring and regenerative braking.
(b) A 220 V, 750 rpm, 60 A dc shunt motor has an armature resistance of 0.2 Ω when running under rated conditions; the motor is to be braked by plugging with armature current limited to 75 A. What external resistance should be connected in series with the armature? Calculate the initial braking torque and its value when the speed has fallen to 600 rpm.

4 (a) Discuss with the suitable diagrams I quadrant and II quadrant choppers.
(b) A 220 V, 24 A, 1000 rpm separately excited dc motor having an armature resistance of 2 Ω is controlled by a chopper. The chopping frequency is 500 Hz and the input voltage is 230 V. Calculate the duty ratio for a motor torque of 1.2 times rated torque at 500rpm.

5 State and discuss various methods of speed control of induction motors.

6 (a) Explain the conditions under which load commutation for CSI can be applied.
(b) A 3-phase, 50 KW,1475 rpm,420 V, 50 Hz, 4-pole star connected induction motor has the following data: R_S=0.4 ohm, R_r=0.21 ohms, X_S=0.95 ohm, X_r=0.85 ohm and X_m=32 ohm, all quantities referred to stator side. If the frequency is increased to 58 Hz by frequency control, determine: i) The slip at maximum torque. (ii) The speed at maximum torque. iii) The break down torque.

7 Write short notes on the following:
(a) Static scherbius drive.
(b) Static kramer drive.

8 (a) Explain the braking in synchronous motors.
(b) What do you mean by ‘AC commutatorless motor’? Explain.

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III B. Tech II Semester (R09) Regular Examinations, April/May 2012

POWER SYSTEM ANALYSIS

(Electrical & Electronics Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
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1 (a) Define and explain the following:
(i) Tree.
(ii) Co – Tree.
(iii) Cut set.

(b) Obtain admittance matrix from basics using singular transformation.

2 Using building algorithm construct Z_{Bus} for the network whose line data is given below. Take bus 2 as reference bus.

Element	self impedance	
	Bus Code	Reactance(p. u)
1	1-2	0.3
2	2-3	0.4
3	1-3	0.3
4	1-4	0.2
5	3 -4	0.5

3 Derive the basic equations for load flow studies and also write the assumptions and approximations to get the simple load flow equations.

4 Draw and explain flow chart for NR method of load flow of a power system.

5 (a) Explain the current limiting reactors in power systems.
(b) Find the reactance of the current limiting reactor external to a 20 MA, 10 kV, 50 Hz, 3 Φ generator such that the steady state current on short circuit shall not exceed 8 times the full-load current. The internal reactance of the generator is 5%.

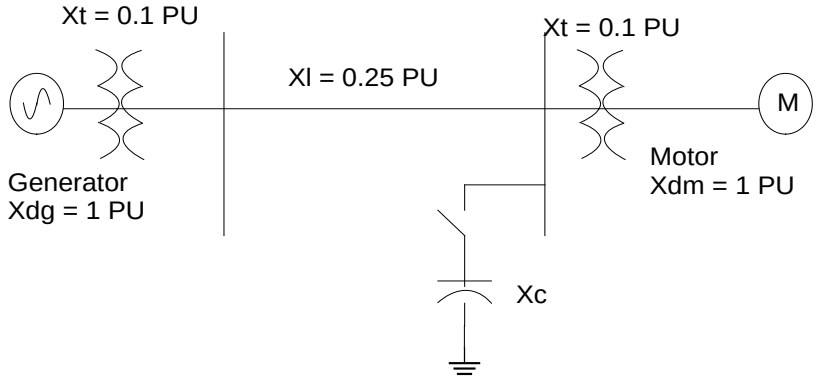
6 What are the methods of improving transient stability?

Contd. in Page 2

7 Two 25 MVA, 11 kV synchronous generators are connected to a common bus bar which supplies a feeder. The star point of one of the generator is grounded through a resistance of 1.0 ohm, while that of the other generator is isolated. A line-to-ground fault occurs at the far end of the feeder. Determine:
(a) The fault current;
(b) The voltage to ground of the sound phase of the feeder at the fault point; and
(c) Voltage of the star point of the grounded generator with respect to ground.
The impendence's to sequence currents of each generator and feeder are given below:

	Generator (per unit)	Feeder (Ω/phase)
Positive Sequence	J0.2	j.04
Negative Sequence	J0.15	J0.4
Zero Sequence	J0.08	J0.8

8 In the system shown below a three phase static capacitive reactor of reactance 1 P.U. per phase is connected through a switch at motor bus bar. Calculate the limit of steady state power with and without reactor switch closed.



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Code: 9A02602

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

POWER SYSTEM ANALYSIS

(Electrical & Electronics Engineering)

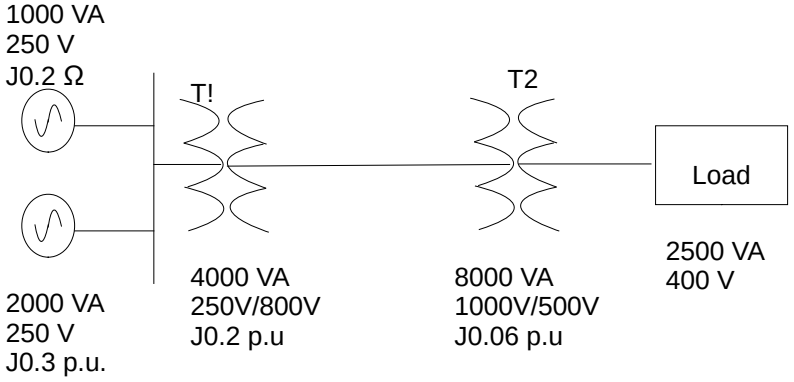
Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 A delta connected resistive load of 15 ohm, 20 ohm and 250 ohm are connected across a balanced three phase supply of 400 V. Find the symmetrical components of line currents and delta currents.

2 A synchronous motor is drawing 30% of the maximum steady state power from an infinite bus bar. If the load on motor is suddenly increased by 100%, would the synchronism be lost. If not, what is the maximum excursion of torque angle about the new steady state rotor position.

3 A simple power system is shown in figure below. Redraw this system where the P.U. impedances are represented on a common base of 5000 VA and 250 V.



4 Discuss the importance of the power system stability study and also briefly express the methods to improve stability.

5 Explain the procedure to form Y_{Bus} by any one method with suitable example.

6 Derive the expressions for building Z_{Bus} when a new element (p-q) is added such that the size of Z_{Bus} will not change. Assume that the added element p-q is mutually coupled with one or more elements of the partial network.

7 (a) Explain Gauss – Seidel method of load flow solution with flow chart.
(b) Explain the classification of various buses in load flow analysis and describe the need for reference bus.

8 Describe fast decoupled load flow method and give algorithm steps of it.

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Code: 9A02602

3

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

POWER SYSTEM ANALYSIS

(Electrical & Electronics Engineering)

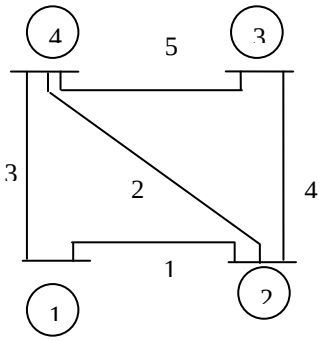
Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 Prove $Y_{br} = KY_{Bus}K^t$ using non-singular transformation.

2 Using building algorithm, construct Z_{Bus} for the system whose data is given below. Choose bus 4 as reference.

Element	Self		Mutual	
	Bus code	Impedance	Bus code	Impedance
1	1-2	j0.5	1-2	j0.2
2	1-4	j0.4		
3	2-3	j0.3		
4	2-4	j0.5		
5	3-4	j0.2		



3 (a) What is slack bus? How do you select a slack bus in a given system?
(b) With the help of flow chart, explain G – S method of load flow solution with PQ buses.

4 Draw the flow chart of decoupled method and explain.

5 (a) Explain bus bar reactors with a neat sketch.
(b) Explain the significance of thevining theorem in fault calculations with an example.

6 What do you mean by term stiffness of synchronous machine? Discuss how a power system's steady state stability can be assessed with this.

7 What is critical clearing angle? Derive the mathematical expression for critical clearing angle.

8 Show that the fully transposed mutually coupled transmission line can be observed in decoupled form in it's sequence circuit.

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Code: 9A02602

4

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

POWER SYSTEM ANALYSIS

(Electrical & Electronics Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 What are the advantages of Z_{Bus} building algorithm? Explain what are primitive network, primitive admittance matrix and primitive impedance matrix. Explain by giving an example.

2 Form Y_{Bus} for the network whose data is given in Table (take bus 1 as reference)

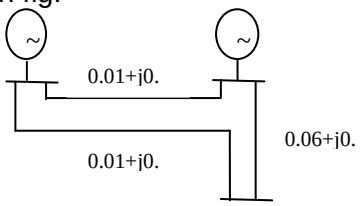
Element	Self		Mutual	
	Bus code	Impedance	Bus code	Impedance
1	1-2	0.6	1-2 (1)	0.2
2	1-2	0.4		
3	1-3	0.5		
4	2-4	0.2	2-4(4)	0.1
5	2-4	0.4		
6	3-4	0.5		

3 Perform one iteration of GS method for the system shown in fig.

Slack bus-1: V=1.05+j0.0

PV Bus-2: $|V_2|$=1.03 p.u., P_2=0.5pu, $0.1<Q_2<0.3$

Load bus-3:P_3=0.6pu, Q_3=0.25pu.



4 Derive an expression for Jacobian elements to carryout load flow study on power system using NR method.

5 (a) Draw the generator equivalent circuit for sub transient and transient periods.
(b) Derive an expression for the fault current for the 3 ø fault.

6 Discuss in detail the methods to improve the steady state stability of a power system.

7 A synchronous generator represented by a voltage source of 1.05 PU in series with a transient reactance of j0.15 PU and in inertia constant H = 4.0 sec. is connected to an infinite inertia system through a transmission line. The line has a series reactance of j0.30PU, while the infinite inertia system is represented by a voltage source of 1.0PU in series with a transient reactance of j0.20 PU.

The generator is transmitting an active power of 1.0 PU when a 3 Φ fault occurs at its terminals. If the fault is cleared in 100 millisecond determine if the system will remain stable by calculating the swing curve.

8 Discuss the various types of unsymmetrical faults that occur in power systems.

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Code: 9A02603

1

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

POWER SYSTEM OPERATION & CONTROL

(Electrical & Electronics Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 Distinguish between incremental fuel cost and incremental production cost for a thermal power plant.

2 The fuel cost functions in Rs/hr for two thermal plants are given by:
$C1=420+9.2P_1+0.004P_1^2$.
$C2=350+8.5P_2+0.0029P_2^2$.
Where P1, P2 are in MW. Determine the optimal scheduling of generation if the total load is 640.82 MW. Estimate value of λ =12Rs/MWh. The transmission power loss is given by the expression $P_{L(pu)}=0.0346P_{1(pu)}^2+0.00643P_{2(pu)}^2$.

3 Describe the objective function to minimize the cost of generation of hydro thermal scheduling.

4 How do the governor characteristics of the prime mover affect the control of system frequency and system load?

5 Two power stations A and B are interconnected by a tie line and have power frequency constants of K_A and K_B MW per Hz. An increase in load of 500 MW on system A causes a power flow of 300 Mw from B to A. When the tie line is open, the frequency of system A is 49 Hz and of B is 50 Hz. Determine the values of K_A and K_B. Derive any formulae used.

6 Draw the block diagram of proportional plus integral controller and show the steady state frequency error is zero.

7 (a) Explain about series compensations. What are the limitations?
(b) Explain the difficulties with an uncompensated line.

8 (a) What is the need of deregulation?
(b) What is the role of modern technology in deregulated power market?

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Code: 9A02603

2

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

POWER SYSTEM OPERATION & CONTROL

(Electrical & Electronics Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 Explain the advantages of competitive electricity market.

2 (a) Why voltage is more sensitive against reactive power than active power?
(b) List out the different power system components and categorize them into reactive power sources and sinks.

3 For a two area frequency control employing integral of area control error, obtain an expression for steady values of change in frequency for unit step disturbance in one of the areas. Assume both areas to be identical. Comment upon the stability of the system for parameter values given below:
T_{SG}=0.4 s ; T_t=0.5s; T_{ps}=20s; K_{ps}=100; R=3; K_i=1; b= 0.425; a_{12}=1; $2\pi T_{12}$=0.05

4 For an isolated power system, the following is the system data:
Rating of the generator =P_r= 100 MW.
Nominal operating load = P_d=50 MW.
Inertia Constant = 5 KW-sec/KVA.
Speed Regulation of the governor = 2.5 Hz/pu MW.
System frequency = 50 Hz.
If the load would increase 1% for 1% frequency increase, find the static frequency change for uncontrolled case when the load is increased by 10 MW. Also find in what proportion the increase in load demand is met by the increase in generation and decrease in load due to drop in frequency.

5 What are the methods of scheduling of generation of steam plants? Explain their merits and demerits.

6 Obtain the condition for optimum operation of a power system with 'n' plants when losses are considered.

7 Explain the mathematical formulation of long-term hydro thermal scheduling.

8 Explain the characteristics of a typical governor of a steam turbine.

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Code: 9A02603

3

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

POWER SYSTEM OPERATION & CONTROL

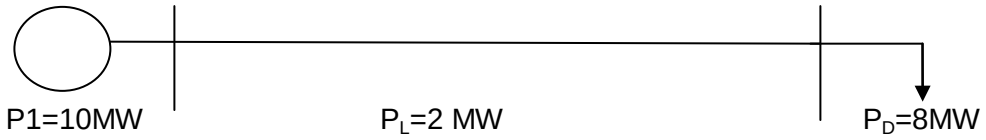
(Electrical & Electronics Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 The cost curves of two generators may be approximated by second degree polynomials:
$C_1=0.1\ P_1^2+20P_1+\alpha_1$
$C_2=0.1\ P_2^2+30P_2+\alpha_2$
Where α_1 and α_2 are constants?
If the total demand on the generators is 200 MW, find the optimum generator settings. How many rupees per hour would you lose if the generators were operated about 15% of the optimum settings?

2 Determine the incremental cost of received power and the penalty factor of the plant shown in figure if the incremental cost of production is dC1/dP1=0.1P1+3.0 Rs/MWh



3 A thermal station and a hydro station supply an area jointly. The hydro station is run 12 hr daily and the thermal station is run throughout 24 hr. The incremental fuel cost characteristic of the thermal plant is $C_T=3+5P_{GT}+0.02\ P_{GT}^2$ Rs. /hr. If the load on the thermal station, when both plants are in operation, is 250 MW, the incremental water rate of the hydro power plant is $dw/dP_{GH}=24+0.004P_{GH} m^3$ /MW-s. The total quantity of water used during the 12 hr operation of a hydro plant is 450 million m^3. Find the generation of hydro plant and the cost of water used. Assume that the total load on the hydro plant is constant for 12 hr period.

4 Explain about non-reheat type of steam turbines.

5 Write short notes on:
(a) Control area. (b) Load frequency control. (c) Voltage control.

6 (a) Explain how the integral controller in load frequency control forms secondary loop.
(b) Explain how the initial droop in frequency is limited in load frequency control.

7 (a) What is series compensation? Explain.
(b) Explain the different aspects of design of series compensator.

8 Explain the problems associated with power pools in deregulation.

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Code: 9A02603

4

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

POWER SYSTEM OPERATION & CONTROL

(Electrical & Electronics Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 Explain about reliability, power quality and pricing issues in deregulated market.

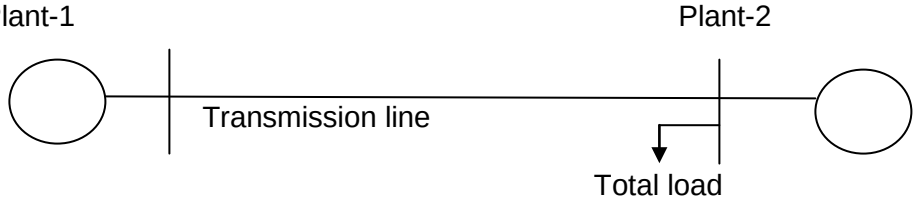
2 (a) Why Ferranti effect is seen in long lines?
(b) Explain the importance of reactive power in electromechanical energy conversion.

3 Explain the loop response of an ALFC system with proportional plus integral controllers.

4 Two generating stations A and B have full load capacities of 200 MW and 75 MW respectively. The interconnector connecting the two stations has an induction motor (plant C) of capacity 25 MW. The % changes of speeds of A, B and C are 5, 4 and 3 respectively. The loads at generating stations A and B are 75 Mw and 30 MW respectively. Determine the load taken by the station 'C and indicate the direction of power flow.

5 Explain the various factors to be considered in allocating generation to different power stations for optimum operation.

6 A system consists of two power plants connected by a transmission line. The total load located at plant-2 is as shown in fig. Data of evaluating loss coefficients consist of information that a power transfer of 100 MW from station-1 to station-2 results in a total loss of 8 MW. Find the required generation at each station and power received by the load when λ of the system is Rs.100 /MWh. The IFCs of the two plants are given by dC1/ dP1 =0.12P1+65 Rs/MWh ; dC2/dP2=0.25P2+75 Rs/MWh.



7 Write the advantages of operation of hydro thermal combinations.

8 Explain about Reheat type of steam turbines.

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Code: 9A04602

1

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

MICROPROCESSORS & MICROCONTROLLERS

(Common to EEE, ECE, CSE, EIE & E. Con. E)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) Briefly explain the internal architecture of MCS-96.
(b) Discuss about the process memory map of MCS-96.

2 (a) What are the advantages of memory segmentation in 8086 microprocessor?
(b) Discuss in brief about assembler directives.

3 (a) Write an ALP in 8086 to find the largest and smallest of a set of 8-bit numbers.
(b) Write an ALP in 8086 to add two ASCII numbers.

4 (a) Draw the block diagram of 8237 & explain its interfacing to 8086 microprocessor with a neat sketch.
(b) Briefly explain the maximum mode configuration of 8086.

5 Sketch and explain the interface of PPI 8255 to the 8086 microprocessor in minimum mode. Interface four 7 segment LEDs to display as a BCD counter.

6 (a) A terminal is transmitting asynchronous serial data at 1200 bd. What is the bit time? Assuming 8 data bits, a parity bit and 1 stop bit how long does it take to transmit one character.
(b) Draw necessary circuit to interface 8251 to an 8086 based system with an address 0C0H. Write the sequence of instructions to initialize 8251 for synchronous transmission. (Assume the necessary data).

7 (a) Draw the block diagram for multiple 8259A based interrupt system.
(b) Explain about cascading of 8259s and its functioning.

8 (a) What is microcontroller? List the features of 8051 microcontroller. Name the five interrupt sources of 8051.
(b) Write an assembly language program in 8051 to find the GCD of two numbers.

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Code: 9A04602

2

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

MICROPROCESSORS & MICROCONTROLLERS

(Common to EEE, ECE, CSE, EIE & E. Con. E)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) Explain the architecture of 8086 microprocessor.
(b) Explain the segmentation in 8086 microprocessor. What are the different registers used for this purpose?

2 (a) Write an ALP to generate the FIBONOCI series.
(b) Write an ALP in 8086 to find 1's complement of a 16 bit hexadecimal number.

3 Explain 8257 DMA interface to 8086 micro processor & what are the registers available in 8257? What are their functions?

4 (a) Explain the functional diagram of 8279 keyboard and display controller.
(b) Discuss about DOS and BIOS interrupts.

5 (a) Explain IOCO and IOSO register for timer 1 in 80196.
(b) What are the interrupt sources for synchronous serial transmission and reception in 80196? What are the identification flags and local enable bits for these sources?

6 Distinguish between Asynchronous and Synchronous data transfer schemes & explain block diagram IC 8251. Explain the logic of 8251 program.

7 (a) With neat diagrams explain the five modes of operation of 8253 in detail.
(b) Draw the block diagram of 8253 and explain about each block in detail.

8 (a) What is assembly language program? What is the function of SWAP?
(b) List out the steps involved in programming the 8051 to transfer data serially.

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Code: 9A04602

3

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

MICROPROCESSORS & MICROCONTROLLERS

(Common to EEE, ECE, CSE, EIE & E. Con. E)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1		Explain the instruction set of 8051 microcontroller. Write a program in 8051 to perform multiplication of two numbers using 8051.
2		Explain about addressing modes and instruction set of MCS-96 family.
3	(a)	Write in detail about the addressing modes of 8086 microprocessor.
	(b)	What are various types of procedures? Give examples.
4	(a)	Write a program to initialize 8251 in synchronous mode with even parity, single SYNCH character, 7 bit data character. Then receive FFH bytes of data from a remote terminal and store it in the memory at address 5000 H: 2000 H.
	(b)	Why are the two ground pins on an RS-232C connector not just jumpered together?
5	(a)	Explain need and importance of DMA.
	(b)	Discuss about Static RAM & EPROM with reference to 8086.
6	(a)	Sketch the interfacing of PPI 8255 to the microprocessor.
	(b)	Interface four 7 segment LEDs to display as a BCD counter.
7	(a)	It is necessary to serve 18 interrupt requests using 8259's. The address map for the 8259's is given from 0A00H to 0A0FH. Show the complete interface with 8086 system bus. These 18 interrupts are to be requested from interrupt type 040H on words, with edge trigged mode and auto end of interrupt. Give the initialization sequence for all 8259's.
	(b)	Explain the operating modes of 8259.
8	(a)	Write an ALP in 8086 to add five 8 bit numbers and the result is 16 bit.
	(b)	Write an ALP in 8086 to add two 8 bit decimal numbers.

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Code: 9A04602

4

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

MICROPROCESSORS & MICROCONTROLLERS

(Common to EEE, ECE, CSE, EIE & E. Con. E)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
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1 (a) Explain the advantages of using the USART chips in microprocessor based systems.
(b) Discuss how 8251 is used for serial communication of data.

2 (a) Explain the flag register of 8086.
(b) Explain the concept of memory segmentation.

3 (a) Write about interrupt sequence in an 8086 system.
(b) Explain about command words of 8259.

4 (a) Write a recursive routine to evaluate the following polynomial Y = A0+A1X+A2X2+A3 X3 +.....+ANXN The coefficients A0,A1,A2....AN are to be successive words in memory and all parameter addresses are to be passed via the stack.
(b) Write a FAR procedure SER WORD that searches a word array for a given word and sets the value of a word parameter to the index of the element in the array if a match is found; otherwise, it puts a -1 in the index word parameter. The parameters are to be passed to the procedure via a parameter address table. Give a sequence for calling SER WORD to search ARRAY 1 of length LENGTH 1 for variable 'ID' and put the index in INDEX 1.

5 What is the difference between minimum and maximum modes of 8086 and also explain how 8086 microprocessor can be configured in minimum and maximum modes of operations?

6 (a) Explain in brief about programming timer interrupts in 8051.
(b) Discuss the bit format of IP register of 8051.

7 (a) Explain the advantages of using the keyboard and display controller chips in microprocessor based system.
(b) Write a program using RST 5.5 interrupt to get an input from keyboard and display it on the display system.

8 (a) Explain the historical perspective in development of MCS - 96 family.
(b) Explain the register to register architecture concept of MCS – 96 family.

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Code: 9A10504

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

LINEAR & DIGITAL IC APPLICATIONS

(Electrical & Electronics Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
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1 (a) List and explain the function of all the basic building blocks of an op-amp.
(b) Mention the reasons why open loop is not preferred for linear applications.
(c) Discuss why negative feedback is desirable in amplifier applications.

2 (a) What are the important features of regulated power supply?
(b) Explain in detail about fixed voltage regulators.
(c) Using 7805 voltage regulator, design a current source to deliver 400mA current to a 50 Ω, 5 W load.

3 (a) Draw the circuit diagram for a fourth order low pass Butterworth filter.
(b) An ideal low pass filter having f_H=5 kHz is cascaded with high pass filter having f_L=4.8 kHz. Sketch the frequency response of the cascaded filter.

4 (a) What is the use of demodulator in a communication system? What is the advantage of FSK?
(b) Explain about following terms with the help of block diagrams using PLL:
(i) Frequency multiplication. (ii) Frequency translation.

5 (a) Explain the operation of R-2R ladder type DAC and the weighted resistor type DAC.
(b) Explain the operation of basic sample and hold circuit.

6 (a) How is propagation delay improved in totem – pole TTL logic?
(b) Explain the working of a two inputs TTL NAND gate with the help of a circuit diagram.

7 (a) Design a 2-bit comparator using logic gates.
(b) Design and implement 8:1 multiplexer using suitable IC's.

8 (a) Design a conversion circuit to convert a D flip - flop to J-K flip - flop.
(b) Explain the internal structure of 64 K x 1 DRAM with the help of timing wave forms discuss DRAM access.

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Code: 9A10504 2

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

LINEAR & DIGITAL IC APPLICATIONS

(Electrical & Electronics Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) What are the advantages of active filters over passive filters?
(b) Define Bessel, Butterworth and Chebyshev filters, and compare their frequency response.
(c) Sketch the circuit diagram of band elimination filter and design a wide band- reject having f_H=200Hz and f_L=1KHz. Assume necessary data.

2 (a) Explain about IC PLL 565 pin diagram.
(b) Perform the closed loop analysis of PLL and derive the transfer function of PLL.
(c) An FM signal is being modulated over the range of 1 MHz ±10 kHz with a modulating frequency of 1 kHz. Design a circuit using PLL to demodulate such a signal.

3 (a) Classify the ICs for a wide range of application with respect to the device used and chip complexity.
(b) Advantages of ICs over discrete component approach to electronics.
(c) What are the three operating temperature ranges of the ICs?

4 (a) What practical modifications to be done to the ideal integrator and why?
(b) Explain the operation of practical op-amp integrator circuit.
(c) Derive the frequency response of practical op-amp integrator.

5 Explain the principle of operations:
(a) Single slope ADC converter. (b) Dual slope ADC converter.

6 (a) Explain CMOS inverter gate with a circuit diagram.
(b) With the help of a neat diagram, explain the working of a two inputs CMOS NAND gate. What is the advantage of active load?

7 (a) Design a 16-bit comparator using 74 X 85 ICs.
(b) With logic diagram and truth table explain the working of 3 to 8 line decoder.

8 (a) Distinguish between synchronous and asynchronous sequential circuits.
(b) Write short notes on static RAM.

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Code: 9A10504

3

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

LINEAR & DIGITAL IC APPLICATIONS

(Electrical & Electronics Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) Explain the terms:
(i) Frequency scaling (ii) Roll of factor and (iii) Damping coefficient.
(b) Explain the working of a band pass filter with its frequency response curve.

2 (a) What is operating principle of PLL? Explain the basic architecture of PLL and explain about each block.
(b) List the applications of PLL.

3 (a) Discuss the non-ideal DC characteristics of an op-amp.
(b) Differentiate between differential gain and common mode gain.
(c) If an op-amp has a common mode rejection ration of 80 dB. If the differential gain is 106 dB, determine the common mode gain.

4 (a) What is a precision diode? Describe the working principle of full wave rectifier using an op-amp with wave forms. Explain how it gives the average value.
(b) What is a clipper circuit? Explain the operation of both positive and negative clippers.

5 (a) Explain the working of 3-bit parallel comparator A/D converter.
(b) A D/A converter have a full scale analog output of 10v and accept 6 binary bits as inputs. Find the voltage corresponding to each analog step.

6 (a) Explain how to estimate sinking current for low output and sourcing current for high output of CMOS gate.
(b) Analyze the fall time of CMOS inverter output with RL = 100, VL = 2.5 V and CL = 10 PF. Assume V_L as stable state voltage.

7 (a) Design a BCD to excess -3 code converter using binary parallel adder.
(b) What is drawback in binary parallel adder? How can it be rectified?
(c) Design a 2-bit magnitude comparator.

8 (a) Realize the logic function performed by 74 × 381 with ROM.
(b) Draw the logic diagram of 74 × 163 binary counter and explain its operation

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Code: 9A10504

4

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

LINEAR & DIGITAL IC APPLICATIONS

(Electrical & Electronics Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) Explain the feedback oscillator principles.
(b) Draw the schematic diagram of a Wien bridge oscillator and explain the operation.
(c) A Wien bridge oscillator uses $R = 4.7\ \mathrm{K\Omega}$, $C = 0.01\ \mu\mathrm{F}$ and $R_f = 2\,R_1$. What is the frequency of oscillation?

2 (a) What is timer IC 555? Draw the internal structure of IC 555 timer.
(b) With the help of equivalent circuit for timing circuit of portion of the 555 monostable circuit and analyze the circuit.

3 Explain different methods of external frequency compensation in an op-amp.

4 (a) What is the purpose of sample and hold circuit? Explain the working principle of sample a hold circuit using an op-amp.
(b) Differentiate clipper and clamper circuit, mention one application of each circuit.

5 (a) Define the term accuracy of DACs. Find the accuracy of 4-bit DAC if the true value of a voltage level is 12V. and its measured value using instrument is 11.9V.
(b) Determine the output voltage of R-2R DAC due to MSB.
(c) Find the resolution of a 4 stage ADC.

6 (a) Mention the DC noise margin levels of ECL 10K family.
(b) A single pull-up resistor to +5 V is used to provide a constant-1 logic source to 15 different 74LS00 inputs. What is the maximum value of this resistor? How much high state DC noise margin can be provided in this case?

7 (a) Design a full subtractor using 3:8 decoders.
(b) Design an odd parity generator for a 4-bit message code.

8 (a) Explain the necessity of two-dimensional decoding mechanism in memories.
(b) Design a modulo-100 counter using two 74 X 163 binary counters.

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Code: 9AHS701

1

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

MANAGEMENT SCIENCE

(Common to Electrical & Electronics Engineering & Electronics & Computer Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 Compare contrast the Fayol's principals of management and Taylor's scientific management theory.

2 What factor do you keep in mind for decentralization and what are its merits and demerits?

3 Give the applications of:
(a) R charts.
(b) P charts.
(c) "C" Chart.

4 (a) Describe the various stages of product life cycle.
(b) Explain how strategies keep changing in time with changes in the stages of product life cycle.

5 What environmental change will be the most difficult for HR group to manage?

6 (a) What is critical path? What is its importance?
(b) Explain the significant information revealed by PERT.

7 What are the internal factors that need to be examined for the firm to assess its strengths and weaknesses?

8 (a) Explain the various terms associated with MRP.
(b) What are the inputs of MRP?

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Code: 9AHS701

2

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

MANAGEMENT SCIENCE

(Common to Electrical & Electronics Engineering & Electronics & Computer Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 What do you mean by strategic alliances? Explain any two forms of strategic alliance.

2 Describe how Indian companies achieve strategic fit between supply chain strategy and competitive strategy in this era of globalization.

3 For the particulars of a project shown in the table below:
(a) Draw a PERT network. (b) Determine critical path. (c) Determine the probability of completing the project within 72 days.

Predecessor Event-Successor event	t_o	t_m	t_p
10-20	6	10	14
10-30	2	4	6
20-50	12	16	24
30-40	16	24	34
40-50	0	0	0
50-80	10	14	18
40-60	12	18	24
40-70	6	12	16
60-90	2	4	6
80-90	6	12	16
70-100	16	30	50
90-100	4	8	12

Normal deviate z and probability values from Normal distribution function table are:

Z	0.6	0.8	1.0	1.2	-0.6	-0.8	-1.0	-1.2
Probability	72.6	78.8	84.1	88.5	27.4	21.2	15.9	11.5

4 What is man power planning? Distinguish between “Man Power Inventory”, “Man Power Skill Inventory” and man power audit.

5 Define management. Explain the nature & scope of management.

6 What is matrix organization and what is uniqueness?

7 Briefly explain various methods of production.

8 Explain the functions of materials manager.

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Code: 9AHS701

3

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

MANAGEMENT SCIENCE

(Common to Electrical & Electronics Engineering & Electronics & Computer Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 Discuss the concept, role and utility of ABC analysis as applied to inventory control.

2 What is the significance of correct plant layout? What are its uses? Which method do you suggest for the efficient plant layout?

3 What is an organizational chart? What does and what does not an organization chart reveal?

4 If you are appointed as a manager in a medium sized manufacturing company, what activities do you have to perform? Explain.

5 (a) Explain the principles of job evaluation.
(b) What is the role of a personnel manager in an organization?

6 The job of a project with respective time estimates are given in table:

Jobs	Optimistic time	Most likely time	Pessimistic time
1-2	3	6	15
1-6	2	5	14
2-3	6	12	30
2-4	2	5	8
3-5	5	1	17
4-5	3	6	15
6-7	3	9	27
5-8	1	4	7
7-8	4	19	28

(a) Draw the network and calculate the following:
(i) Variance of each job. (ii) Length of the project (iii)Variance of project
(b) What is the probability that the jobs on the critical path will be completed by the due date 42 days?

7 Discuss the stages in the strategy formulation and implementation. Explain.

8 What is Supply Chain Management? What are the benefits of SCM?

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Code: 9AHS701

4

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

MANAGEMENT SCIENCE

(Common to Electrical & Electronics Engineering & Electronics & Computer Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 Explain the following terms in reference to quality control:
i) Producer's risk. (ii) Consumer's risk.
iii) Average outgoing quality. (iv) Single sampling plan of inspection.

2 Do you agree with the statement "A company should go in for available internal skills and a policy of promotion from with always". Justify.

3 Given the following information workout the minimum duration of the project and the corresponding cost.

Activity	Job	Normal time (days)	Crash time (days)	Normal cost (Rs)	Crash cost (Rs)
A	1-2	10	6	400	600
B	1-3	4	2	100	140
C	2-4	6	4	360	440
D	3-4	8	4	600	900
E	2-5	8	6	840	1100
F	4-6	6	2	200	300
G	5-6	10	8	1200	1400

4 What do you mean by transfer? Explain the essentials of a good transfer policy. And also explain different types of transfers.

5 Explain the Mc. Gregore's theory of -`X' and theory – Y.

6 What are the principles of sound organization structure? Explain.

7 (a) What are the objectives of plant layout?
(b) Explain the factors influencing plant layout.

8 Define management. Explain its functions.

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Code: RE 9A10504

1

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

LINEAR & DIGITAL IC APPLICATIONS

(Electrical & Electronics Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) Explain common mode voltage, common mode voltage gain, and common mode rejection ratio for operational amplifiers.
(b) An operational amplifier circuit with a closed loop gain of 100 has a common mode output of 5 μV when the common mode input is 10 mV. Determine common mode rejection ratio. Also calculate the power supply rejection ratio if 1 μV supply ripple is present at the output of the op-amp when the supply voltage has a 25 mV ripple.

2 (a) Sketch the logarithmic amplifier circuit using OP-AMP, and explain its operation with suitable expressions.
(b) What is anti-logarithmic amplifier? Discuss the operation of the circuit by giving necessary expressions.

3 (a) Draw the internal block diagram of 555 timer IC and explain the importance of every component/block of it.
(b) With help of suitable sketches, how 555 timer IC can be used as a monostable multivibrator.

4 (a) Explain the operation of CMOS inverter with suitable diagram(s).
(b) Give the generalized NOR structure using CMOS with multiple inputs, and explain its operation.

5 (a) With suitable diagrams and expressions, explain the TTL to CMOS level shifting of voltages.
(b) Give the comparison of Logic families of TTL and CMOS.

6 (a) What are the behavioral design elements in VHDL? Explain them.
(b) Describe a simple inverter with feed back in VHDL.

7 (a) Design a 3 input 5-bit multiplexer. Write the truth table and draw the logic diagram.
(b) Write short notes on full subtractor.

8 (a) Convert T flip-flop by adding external gates to a D flip-flop with clock enable.
(b) Design a 4-bit binary synchronous counter using 74×74.

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Code: RE 9A10504 2

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

LINEAR & DIGITAL IC APPLICATIONS

(Electrical & Electronics Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) Draw the ac equivalent circuit for the dual input and balanced output differential amplifier and derive the expressions for the differential input resistance, output resistance and voltage gain for the same.
(b) What is the importance of current mirror circuit used in OP-AMP? Explain the same with suitable sketches.

2 (a) Design a non-inverting Schmitt trigger circuit to have UTP = +3 V, and LTP = -5 V. Use a 741 OP-AMP with V_{CC} = ±15 V, and assume suitable data.
(b) Draw the OP-AMP based astable multivibrator circuit, and explain its functionality in detail.

3 (a) List out important features of 555 timer IC. What are the two modes in which the 555 timer is operated?
(b) Design a monostable multivibrator circuit using 555 timer for the following specifications: Frequency of the output waveform: 5 kHz, Duty cycle: 40%, peak – to – peak amplitude of the output waveform is 5 V. Assume necessary data.

4 (a) With suitable sketches, explain the operation of CMOS two input NAND gate.
(b) Give the CMOS steady state electrical behavior.

5 (a) Describe the operation of a totem pole configuration of TTL logic circuit with suitable circuit diagram.
(b) Why the emitter coupled logic circuit is fastest of all logic circuits? Explain. Give the circuit diagram of ECL circuit and explain its operation.

6 (a) Give the VHDL description for a two input NAND gate whose output is connected to one of the inputs of a two input OR gate.
(b) List out the functions and procedures in VHDL.

7 Write the following:
(a) Design procedure for EX-OR gate
(b) Design procedure for even parity generator circuit.

8 (a) Design an 8-bit parallel-in and serial-out shift register? Explain the operation of the above shift register with the help of timing waveforms?
(b) Convert by adding external gates (i) a D flip-flop to a J-K flip flop with clock enable.

*****

Code: RE 9A10504

3

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

LINEAR & DIGITAL IC APPLICATIONS

(Electrical & Electronics Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) With the help of circuit diagram, explain the operation of a dual input unbalanced output differential amplifier.
(b) An OP-AMP has a differential gain equal to 100 dB and CMRR is 120 dB. If the two input voltages are 3μV, and 2 μV respectively, calculate the differential mode output and common mode output voltages.

2 (a) Describe the working principle of precision full-wave rectifier with suitable sketches and expressions.
(b) Sketch the circuit of a triangular/rectangular waveform generator. Draw the output waveforms from the circuit showing their phase relationship and explain the circuit operation.

3 (a) Explain the operating principle of phased locked loop (PLL 565) with suitable block diagram. Mention its applications.
(b) State and explain the following terms with reference to phased locked loops: capture range, lock range, and free running frequency.

4 (a) With suitable sketches, explain the operation of CMOS two input NOR gate and its complementary.
(b) Give the CMOS dynamic electrical behavior.

5 (a) With the help of circuit diagram, explain the operation of Emitter Couple Logic gate. List out all its logic levels.
(b) Explain the terms: Fan-in and Fan-out with a suitable example for each of them.

6 (a) Write a complete VHDL module for a two input AND gate whose output is given to a NOT gate.
(b) Explain the terms: Entity declaration and structural description of VHDL. Give suitable examples.

7 Write the following:
(a) Design procedure for 4 bit full adder circuit.
(b) Design procedure for 4 – to - 1 multiplexer.

8 (a) Design a conversion circuit to convert a D flip-flop to J-K flip-flop.
(b) Design a 4-bit binary synchronous counter using 74×74.

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Code: RE 9A10504

4

III B. Tech II Semester (R09) Regular Examinations, April/May 2012

LINEAR & DIGITAL IC APPLICATIONS

(Electrical & Electronics Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) Derive the expressions for input resistance, output resistance, voltage gain of a single input unbalanced output differential amplifier, and compare them with those of the dual input balanced output amplifier.

(b) For a practical dual input balanced output differential amplifier, the component values are: R_{in} = 1 kΩ, R_E = 2.5 MΩ, h_{fe} = 50, h_{ie} = 1 kΩ, and assume other h-parameters of the transistors are zero. The circuit is operated with differential signal of 1mV and common mode signal of 20 mV. Calculate the output voltage and CMRR.

2 (a) Discuss the design process for an OP-AMP inverting Schmitt trigger circuit and write equations for calculating each component value.

(b) A monostable multivibrator circuit is to have a 650 µs, ±9 V output pulse when triggered by a 50 µs, 3 V input pulse. Design the circuit using OP-AMP.

3 (a) Design an astable multi vibrator using 555 timer whose output waveform should have 40% duty cycle.

(b) Discuss about the importance of 565 PLL and explain its operation with respect to one application.

4 (a) Explain how to estimate sinking current for low output and sourcing current for high output of CMOS gate.

(b) Analyze the fall time of CMOS inverter output with R_L = 1 K, V_L = 2.5 V and C_L = 100 PF. Assume V_L as stable state voltage.

5 (a) With help of circuit diagram, explain the operation of a TTL two input NAND gate.

(b) How do you interface CMOS logic gates with that of TTL? Explain.

6 (a) Give the procedure to compile and simulation of VHDL code.

(b) List out different operators used VHDL. Give an example for each of them.

7 Write the following:
(a) Design procedure for EX-OR gate.
(b) Design procedure for odd parity generator circuit.

8 (a) Design a modulo-100 counter using two 74×163 binary counters.

(b) Design an 8-bit parallel-in and serial-out shift register. Explain the operation of the above shift register with the help of timing waveforms.

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