Code: 9A02601

1

B. Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

POWER SEMICONDUCTOR DRIVES

(Electrical & Electronics Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Explain the operation of single phase semi-converter fed separately excited d.c. motor drive with necessary diagrams.

(b) A DC shunt motor operating from a 1-ø half controlled bridge at a speed of 1450 rpm has an input voltage 330 sin 314 t and a back emf 75 V. The SCRs are fired symmetrically at $\alpha = \pi/3$ in every half cycle and the armature has a resistance of 5 Ω. Neglecting armature inductance, find the average armature current and the torque.

2 Describe the use of three phase semi converter for the speed control of a D.C series motor. Illustrate your answer with appropriate waveforms and also derive the rms values of source and thyristor currents.

3 (a) Explain how four-quadrant operation is achieved by dual converters each of 3 φ full wave configuration for d.c. separately excited motor.

(b) Distinguish between circulating current and non-circulating current mode of operation.

4 (a) Distinguish between class A and class B choppers with suitable examples of speed control of motors.

(b) A dc supply of 220 V supplied power to separately excited dc motor via a class A thyristors chopper. The motor has an armature circuit resistance of 0.03 Ω and inductance of 3 mH. The chopper is fully on at the rated motor speed 1200 rpm when the armature current is 50 A. If the speed is to be reduced to 1000 rpm with the load torque constant, calculate the necessary duty cycle.

5 Describe the operation of reversible induction motor drive fed by an ac voltage controller for four quadrants of operation.

6 Explain the operation of voltage source inverter fed induction motor drive with neat diagram.

7 (a) State the major features of rotor resistance control of wound rotor induction motor.

(b) The speed of a 3-phase slip ring induction motor is controlled by variation of rotor resistance. The full load torque of the motor is 50 N-m at a slip of 0.3. The motor drives load having a characteristic of $T \propto N^2$. The motor has 4 poles and operated on 50 Hz, 400 V supply. Determine the speed of the motor for 0.8 times the rated torque. The operation condition is obtained with additional resistance in the rotor circuit by chopper control. Determine the average torque developed for a time ratio of 0.4.

8 Explain the operation of three pulse midpoint cyclo-converter fed self controlled synchronous motor with the help of neat sketches.

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Code: 9A02601

2

B. Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

POWER SEMICONDUCTOR DRIVES

(Electrical & Electronics Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Explain the operation of single phase fully controlled rectifier fed d.c. series motor with relevant diagrams.

(b) A series motor is supplied from a full converter whose $\alpha = 65^0$, 1-ø supply of 230 V rms, 50 HZ frequency. The armature and field resistance together equal 2 Ω. The torque constant is 0.23 H and the load torque is 20 Nm. Neglect damping and find the average armature current and speed.

2 Explain the speed - torque characteristics of a separately excited dc motor connected to a three phase semi controlled converter.

3 (a) Explain the principle of operation of a dual converter in circulating current mode. How the same is used for speed control of dc drive?

(b) Discuss in detail counter current and dynamic braking operations of D.C shunt motors.

4 (a) Draw and explain in detail of motoring and regenerative braking operation of chopper control of separately excited DC motor.

(b) A 220 V, 24 A, 1000 rpm separately excited dc motor having an armature resistance of 2 Ω is controlled by a chopper. The chopping frequency is 500 Hz and the input voltage is 230 V. Calculate the duty ratio for a motor torque of 1.2 times rated torque at 500 rpm.

5 (a) Using a 3-phase solid state AC voltage controller explain clearly how it is possible to achieve 4-quadrant operation of 3-phase induction motor.

(b) Draw a closed loop speed control scheme of an induction motor with AC voltage controller.

6 Compare VSI and CSI fed induction motor drives.

7 (a) What is the range of firing angle of thyristors in line communicated inveter fed static scherbius drive. Describe in detail.

(b) In a static Kramer drive system of an induction motor how speeds can be controlled from synchronous speed to stand still.

8 Explain the variable frequency control of synchronous motor in detail.

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Code: 9A02601

3

B. Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

POWER SEMICONDUCTOR DRIVES

(Electrical & Electronics Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Explain the concept of constant torque control and constant power control.
(b) Explain how the speed control of a dc motor is achieved illustrating the triggering circuits of the thyristors.

2 A 100 KW, 500 V, 2000 rpm separately excited dc motor is controlled by a three-phase fully controlled converter and is fed from a 400 V, 50 Hz supply. The voltage drop in conducting the thyristor is 2 V. Motor parameters are R_a =0.1 Ω, L_a =8 mH, K_m =1.6. Rated armature current = 210 A. No load current is 10% of rated current.
(a) Find no load speed at firing angle of 30^0.
(b) Find the firing angle to obtain 2000 rpm at rated armature current. Also find supply power factor.

3 With neat circuit diagram and waveforms, explain dynamic braking, regenerative braking and plugging of separately excited motor.

4 (a) Deduce the mathematical expression for minimum and maximum currents for a class A chopper operated dc motor with back emf.
(b) A 220 V, 12 A, 1000 rpm separately excited dc motor having an armature resistance of 2 Ω is controlled by a chopper. The chopping frequency is 200 Hz and the input voltage is 230 V. Calculate the duty ratio for a motor torque of 2 times rated torque at 750 rpm.

5 Explain various speed control methods of induction motor applicable for both squirrel cage and slip ring induction motors.

6 Explain with suitable block diagrams, the various types of VSI controlled induction motor drives.

7 (a) Describe the operation of static scherbius. Drive with a neat schematic.
(b) Why a resistance starter is generally required for the induction motor drive employing slip-power recovery?

8 (a) Explain the advantages and applications of load commutated CSI fed synchronous motors.
(b) Explain the speed torque characteristics.

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Code: 9A02601

4

B. Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

POWER SEMICONDUCTOR DRIVES

(Electrical & Electronics Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Write down the basic performance equations for a D.C Series motor Sketch characteristics of constant torque drive and constant power drive regions.

(b) A 200 V, 1200 rpm, 200 A separately excited DC motor is fed from 1-Φ, fully controlled converter with an ac source 230 V, 50 HZ supply. The thyristor is triggered continuously by a DC signal. The resistance of armature circuit is 0.05 Ω. Find the motor speed for firing angle 90^0 and rated torque.

2 The speed of a separately excited dc motor is controlled by means of a 3 phase semi-converter from a 3 phase 415 V 50 Hz supply. The motor constants are inductance10 mH, resistance 0.9 ohm and armature constant 1.5 v/rad/s. Calculate speed of the motor at a torque of 50 Nm when the converter is fired at 45^0. Neglect losses in the converter.

3 Explain with proper circuit diagram speed-torque characteristics of D.C motor under dynamic braking, for the following types:
(a) Separately excited dc motor.
(b) Series motor.

4 Derive the expressions for average motor current, RMS motor currents, torque and average motor voltage, for chopper fed D.C separately excited motor.

5 Describe the operation of ac voltage controller fed three phase induction motor with neat circuit diagram and waveforms.

6 With help of a neat block diagram, explain the closed loop control of PWM inverter fed Induction motor drive with regenerative braking.

7 (a) What are the advantages of static rotor resistance control over conventional methods of rotor resistance control?

(b) Why has the static Kramer drive a low range of speed control?

8 Explain the closed loop operation of synchronous motor drives with neat sketches.

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Code: 9A02602

1

B. Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

POWER SYSTEM ANALYSIS

(Electrical & Electronics Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Obtain the relationship between number of nodes, number of branches, number of elements and number of links.

(b) Describe any one method to derive bus admittance matrix.

2 Form Z_{Bus} for the network whose data is given in Table (take bus 1 as reference)

Element	Self		Mutual	
	Bus code	Impedance	Bus code	Impedance
1	1-2	0.6	1-2 (1)	0.2
2	1-2	0.4		
3	1-3	0.5		
4	2-4	0.2	2-4(4)	0.1
5	2-4	0.4		
6	3-4	0.5		

3 Why direct simulation of load flow is not possible? And mention data required for load flow solution. Also derive simple load flow equations by considering assumptions.

4 Explain decoupled load flow method to find the solution of a system with the help of flow chart.

5 (a) Determine an expression for fault current and MVA in terms of P.U. impendence.

(b) A 3-Φ 100 MVA, 13.8 KV generator has a subtransient reactance of 15%. Find the MVA_{sc} and I_{sc}.

6 Show that:

(a) The zero sequence components of line voltages are always zero.

(b) In the absence of a neutral connection the zero sequence line current is always zero.

(c) The symmetrical component transformation is power invariant.

7 What do you understand by steady state stability? Discuss in detail about the synchronizing power coefficients.

8 The transfer reactances between a generator and an infinite bus bar operating at 200 K under various conditions on the interconnector are:

Prefault 150 Ω per phase

During fault 400 Ω per phase

Post fault 200 Ω per phase

If the fault is cleared when the rotor has advanced 60 degrees electrical from its prefault position, determine the maximum load that could be transferred without loss of stability.

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Code: 9A02602

2

B. Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

POWER SYSTEM ANALYSIS

(Electrical & Electronics Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 Explain the following:
(a) Cut set matrix. (b) Bus incidence matrix. (c) Branch path incidence matrix.
(d) Basic loop incidence matrix.

2 Derive the expression for building Z_{Bus} when the added element is connected:
(i) Between an existing bus and a new bus.
(ii) Between the reference bus and a new bus.
Assume that the added element is mutually coupled with one or more elements of the partial network.

3 Determine the value of V_2, V_3 and V_4 as produced by the first iteration of the G-S procedure for the data given below (Table 1&2).

Table 1: Line data

Line	R1 (pu)	X1(pu)
1-2	0.05	0.15
1-3	0.10	0.30
2-3	0.15	0.45
2-4	0.10	0.30
3-4	0.05	0.15

Table 2: Load data

V(pu)	P(pu)	Q(pu)	Type of bus
$1.04\angle 0°$	-	-	Slack
-	0.5	-0.2	PQ
-	-1	0.5	PQ
-	0.30	-0.1	PQ

4 Give algorithm steps for fast decoupled load flow method to find the solution of power system.

5 Explain the short circuit phenomenon in 3-$\emptyset$ synchronous generator and draw the oscillogram of short circuit current and show subtransient, transient and steady state currents.

6 Discuss the symmetrical component method to analyze an unbalanced 3-phase system.

7 Discuss the power angle curve of a synchronous machine and also give the classical representation of a synchronous machine in stability studies.

8 Derive the swing equation for a machine connected to an infinite bus in a power network and extend it for a two machine system

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Code: 9A02602

3

B. Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

POWER SYSTEM ANALYSIS

(Electrical & Electronics Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Discuss about steps involved in solving a problem using digital computer.

(b) Derive bus admittance matrix using singular transformation.

2 Derive the necessary equations for modifying Z_{Bus} elements when an element having mutual impedance with one or more elements has been disconnected from the network.

3 Derive fundamental equations for load flow studies and also write the assumptions and approximations to get the simple equations.

4 Explain and derive necessary equations to carry out NR method of load flow solution in polar coordinates.

5 (a) What are the advantages of P.U. system?

(b) A 30 MVA, 11 KV generators has a reactance of 0.2 P.U. referred to its ratings as bases. Determine the P.U. reactance when referred to base KVA of 50,000 KVA and base KV = 22 KV.

6 A synchronous generator is rated 25 MVA, 11 KV. It is star connected with the neutral point solidly grounded. The generator is operating at no load at rated voltage. Its reactances are $X'' = X_2 = 0.20$ and $X_0 = 0.08$ pu. Calculate the symmetrical subtransient line currents for :

(i) Single line to ground fault;

(ii) Double line fault;

(iii) Double line to ground fault; and

(iv) Symmetrical three phase fault.

Compare these currents and comment.

7 How do you broadly define and classify power system stability? Establish the concept of power system stability analytically.

8 What is equal area criterion? Interpret this for a case when there is a sudden short circuit at one end of one of the line of parallel lines.

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Code: 9A02602

4

B. Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

POWER SYSTEM ANALYSIS

(Electrical & Electronics Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 Explain the procedural steps to calculate bus admittance matrix by direct method.

2 How bus impedance matrix is developed by step by step method? Describe the method with algorithm.

3 (a) Explain why voltage vector for a power system is called “State Vector” in load flow analysis. Explain its significance.

(b) Explain the procedure to incorporate Q limits for PV buses in the solution of load flow studies.

4 Draw and explain the flow chart for DC load flow.

5 (a) Explain about fault limiting reactors.

(b) Show that 3-Φ short circuit fault is a symmetrical fault.

6 What do you understand by symmetrical component transformation?

7 A 50 Hz transmission line 500 km long with constants given below ties up two large power areas. R = 0.11 Ω/km, L = 1.45 mH/km, C = 0.009 μF/km, G = 0

(a) Find the steady state stability limit if $|V_S| = |V_R| = 200$ KV (constant).

(b) What will be steady state stability limit be if line capacitance is also neglected? What will be steady state limit if line resistance is neglected?

8 How do you define the transient stability of a power system? How can you model the transmission line, load and alternators in transient stability studies?

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Code: 9A02603

1

B. Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

POWER SYSTEM OPERATION & CONTROL

(Electrical & Electronics Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 Explain the λ-iterative technique used to solve economic load dispatch problem.

2 Two units of a thermal station have each the following cost characteristics C = 5500 + 450 P + 0.5 P^2 Rs/hr. Due to an instrumentation error the cost characteristics of first unit is in error by +2% and that of the second unit by -2% at the time of scheduling. Find the extra operating cost due to erroneous scheduling. Total load is 200 MW.

3 Describe the types of hydro thermal co-ordination.

4 Obtain the derivation of small signal transfer function of speed governing system.

5 Explain the operation of two major control loops ALFC and AVR with the help of a neat block diagram.

6 Draw the complete block diagram of the LFC of an isolated power system with proportional plus integral controlees. Explain about each block.

7 (a) List out different reactive power compensation devices. Explain briefly about them.

(b) Explain why compensator is connected at load end than at generator end in a radial transmission line.

8 Explain the motivation for the restructuring power system.

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Code: 9A02603

2

B. Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

POWER SYSTEM OPERATION & CONTROL

(Electrical & Electronics Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 Draw the flow chart for obtaining optimal scheduling of generating units by neglecting the transmission losses

2 What are the B-coefficients? Derive them.

3 Explain briefly about:
(a) Long term co-ordination.
(b) Short term co-ordination.

4 Draw the schematic diagram of a speed-governing system and explain the function of its components.

5 (a) Distinguish between load frequency control and economic dispatch control.
(b) Explain the dynamic response of ALFC loop with first order approximation.

6 (a) Explain how the proportional controller in load frequency control forms primary loop.
(b) Explain how reset of frequency control is achieved in Load frequency control.

7 Differentiate between series and shunt compensations with proper examples.

8 (a) Explain the models of electricity markets.
(b) What is the role of transmission expansion in deregulated market?

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Code: 9A02603

3

B. Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

POWER SYSTEM OPERATION & CONTROL

(Electrical & Electronics Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 Explain in detail the following for the power system network :
(i) Control variables.
(ii) Disturbance variables.
(iii) State variables.

2 Draw flow chart for optimum operation of a power system with 'n' plants when losses are considered.

3 Explain Kirchmayer's method.

4 Derive transfer function model of speed governing system.

5 Derive the expression for steady state frequency change in a two control area system.

6 For a two area load frequency control with proportional plus integral controller, derive the expression for steady values of change in frequency and tie line power for simultaneously applied unit step load disturbances in the two areas.

7 Explain the need of voltage control in power systems. How it is achieved?

8 Explain the technical issues related to embedded generation in deregulated power market.

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Code: 9A02603

4

B. Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

POWER SYSTEM OPERATION & CONTROL

(Electrical & Electronics Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 Explain the significance of equality and inequality constraints in the economic allocation of generation among different plants in a system.

2 Give a step-by-step algorithm for computing economic allocation of power generation in a thermal system when transmission line losses are considered.

3 In a two plant operation system, the hydro plant is operate for 8 hrs during each day and the steam plant is operate all over the day. The characteristics of the steam and hydro plants are $C_T = 0.025\ P_{GT}^2 + 14\ P_{GT} + 12$ Rs/hr, $W_H = 0.002\ P_{GH}^2 + 28\ P_{GH}$ m^3/sec. When both plants are running, the power flow from steam plant to load is 200 MW and the total quantity of water is used for the hydro plant operation during 8 hrs is 220×10^6 m^3. Determine the generation of hydro plant and cost of water used. Neglect the transmission losses.

4 Explain about the dynamic interaction between P-f and Q-V loops.

5 Two synchronous generators operate in parallel and supply a total load of 400 MW. The capacities of machines are 200 MW and 500 MW and both have frequency droop characteristics of 4% from no load to full load. Calculate the load taken each machine assuming free governor operation. Also find the system frequency at this load.

6 Explain how different gains of integral controller affect the dynamic response of LFC system.

7 Explain how the reactive power is compensated during base loads and peak loads.

8 (a) Explain the advantages of competitive power generation in modern era.

(b) Explain about restructuring of power systems.

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Code: 9A04602

1

III B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2013

MICROPROCESSORS & MICROCONTROLLERS

(Common to EEE, ECE, CSE, EIE & E.Con.E)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Why the lower order address bus is multiplexed with data bus? How they will be de-multiplexed?

(b) Differentiate between maskable and non-maskable interrupts.

2 (a) Write an ALP in 8086 to check the number is prime or not.

(b) Write an ALP in 8086 to convert un packed BCD to packed BCD.

3 (a) Draw the memory write machine cycle in minimum mode and explain the operation in each T state.

(b) Draw and explain the memory write machine cycle in maximum mode.

4 (a) Explain how to interface a stepper motor with 4-step input sequence to 8086 based system with the help of hardware design. Write the instruction sequence to move the stepper motor 10 steps in clockwise and 12 steps in anti-clockwise direction.

(b) Write in detail about stepper motor and actuators and their interface with 8086.

5 (a) What are the applications of 8251? Whether write operation is possible with status word & command word registers.

(b) Distinguish between asynchronous and synchronous data transfer schemes.

6 (a) Draw the block diagram of 8253 and explain about each block in detail.

(b) Explain about control word format and programming of 8253.

7 (a) Explain in brief about programming external hardware interrupts in 8051.

(b) What are the steps involved in programming the 8051 to receive data serially?

8 (a) Explain the importance of each pin in MCS-96 microcontrollers.

(b) Give a short note on 80196 micro controller of MCS-96 family.

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Code: 9A04602

2

III B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2013

MICROPROCESSORS & MICROCONTROLLERS

(Common to EEE, ECE, CSE, EIE & E.Con.E)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Discuss the memory segmentation in 8086 microprocessor.

(b) Briefly explain the architecture of 8086 microprocessor with a neat sketch.

2 Assume that the symbol table starting at location TABLE consists of 100 entries. Each entry has 80 bytes with the first 8 bytes representing the name field and the remaining 72 bytes representing the information field. Write an instruction sequence to search this table for a given name of 8 characters stored in NAME. If the name is found, copy the associated information into INFO, otherwise, fill INFO with null characters.

3 (a) Explain the control pins used in minimum mode operation.

(b) Differentiate minimum and maximum mode of 8086.

4 (a) With neat layout, explain how a microprocessor can be used for data acquisition system using A/D converters and D/A converters.

(b) Explain in detail about the interrupt structure of 8086 microprocessor.

5 (a) What is the significance of SYNC DETECT & BREAK DETECT signals in 8251?

(b) Define command word & status word register of 8251.

6 (a) Draw the pin diagram of 8259 and explain briefly about the function of each pin.

(b) Draw the internal block diagram of 8259 and explain about each block.

7 (a) Write program to load accumulator, DPH & DPL using 8051.

(b) Write short notes on the use of control signals $\overline{WR}$ and $\overline{RD}$.

8 Explain address mapping and memory mapping in detail about MCS-96 micro controllers.

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Code: 9A04602

3

III B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2013

MICROPROCESSORS & MICROCONTROLLERS

(Common to EEE, ECE, CSE, EIE & E.Con.E)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Discuss the various addressing modes of 8086. What are displacement, base and index? What is an effective address or offset?

(b) What are the advantages of the instruction queue in 8086?

2 (a) Write an ALP to separate and count the numbers from positive negative and zero numbers from a given set of 8 bit numbers.

(b) Write an ALP in 8086 to convert packed BCD to unpacked BCD.

3 (a) Explain in brief the need for DMA controller and its working in an 8086 based system.

(b) Differentiate minimum and maximum mode of 8086.

4 (a) Draw the schematic diagram of 8255 PPI and explain different modes of operation of 8255 with example.

(b) Draw the block diagram of 8255 and explain each block.

5 (a) What is parity error, over run error & frame error in 8251? What is hunt mode in 8251?

(b) Explain about USB with necessary example & analysis.

6 (a) Explain the modes of operation of 8253 in detail.

(b) Why do we prefer interrupt driven data transfer than programmed I/O transfer? Show the complete hardware design to resolve the multiple interrupts based on priority.

7 (a) What is assembly language program? What is the function of SWAP? What is debugging?

(b) Write a program to subtract the contents of R1 of Bank 0 from the contents of R0 of Bank 2.

8 (a) Describe about versions and cores of ARM microcontrollers.

(b) Give salient features about ARM microcontrollers.

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Code: 9A04602

4

III B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2013

MICROPROCESSORS & MICROCONTROLLERS

(Common to EEE, ECE, CSE, EIE & E.Con.E)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Write an assembly language program that will examine an ASCII string of 100 characters and replace each decimal digit by a %. The character string starts at STRG.

(b) Explain the prefix instruction format of 8086 processor. Discuss how these instructions are useful in string manipulation.

2 (a) Write an ALP in 8086 to multiply two 16 bit numbers and the result is 32 bit.

(b) Write an ALP in 8086 to add two 8 bit ASCII numbers.

3 (a) What are the registers available in 8257? What are their functions?

(b) Draw and discuss the status registers of 8257.

4 (a) Give the relevant hardware and software for interfacing stepper motor to 8086 based system.

(b) Explain A/D converter interface to 8086 micro processor.

5 (a) Define mode word register of 8251 for asynchronous mode.

(b) Define mode word register of 8251 for sync mode.

6 (a) With neat block diagram explain the functions of 8259.

(b) Explain the programming sequence of PIC along with flow chart explain each command word in detail.

7 (a) Write a program to load accumulator A, DPH and DPL with 30 H.

(b) Write short notes on external interrupts of 8051.

8 (a) What is the difference between Interrupt Request (IRQ) and Fast Interrupt Request (FIQ) in ARM? Explain.

(b) Compare the CPSR and SPSR registers formats and their purpose in different modes of ARM processor operations.

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Code: 9A10504

1

B.Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

LINEAR AND DIGITAL IC APPLICATIONS

(Common to EEE and MCT)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) List out different configurations of differential amplifier.
(b) Compare and contrast an ideal op-amp and practical op-amp.
(c) List out the AC characteristics of an op-amp and discuss about them.

2 (a) Design a differentiator to differentiate an input signal that varies in frequency from $10\ \mathrm{Hz}$ to about $1\ \mathrm{KHz}$. If a sine wave of $1\ \mathrm{V}$ peak at $1000\ \mathrm{Hz}$ is applied to this differentiator draw the output waveforms.
(b) Design a logarithmic amplifier for positive input voltages in the range $5\ \mathrm{mV}$ to $50\ \mathrm{V}$.

3 (a) Draw the block schematic of a PLL describing the function of each block briefly.
(b) Explain the different applications of PLL.

4 (a) Design a 4-input CMOS AND-OR-INVERT gate. Draw the logic diagram and function table.
(b) Distinguish between static and dynamic power dissipation of a CMOS circuit.

5 (a) Compare CMOS, TTL and ECL with reference to logic levels, DC noise margin propagation delay and fanout.
(b) Design a transistor circuit of 2-input ECL NOR gate. Explain the operation with the help of function table.

6 (a) Explain structural design elements of VHDL.
(b) Explain with example the syntax and the function of the following VHDL statements:
(i) Concurrent signal assignment statement
(ii) Selected signal assignment statement
(iii) Port map

7 (a) Using two 74X138 decoders design a 4 to 16 decoder.
(b) Write a data flow style VHDL program for the above design.

8 (a) Explain working of the various programmable logic devices.
(b) Differentiate between ripple counter and synchronous counter. Design a 4-bit counter in both modes and estimate the propagation delay.

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Code: 9A10504

2

B.Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

LINEAR AND DIGITAL IC APPLICATIONS

(Common to EEE and MCT)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Define thermal drift. What is the need for frequency compensation?
(b) Explain the DC characteristics of op-amp.

2 (a) Draw the circuit diagram of a two input non inverting type summing amplifier and derive the expression for output voltage.
(b) Explain the operation of log amplifier using op-amp.

3 (a) Explain the terms lock range, capture range and pull-in time of a PLL.
(b) Design and explain a 555 astable multivibrator to operate at 10 KHz with 40% duty cycle.

4 (a) Explain briefly MOS and CMOS logic families and give different CMOS characteristics.
(b) Draw the circuit of CMOS NOR gate and explain its operation. Mention any two points about the advantages of CMOS over the other digital logic families.

5 (a) Design TTL three state NAND gate and explain the operation with the help of functional table.
(b) Which is the fastest non-saturated logic gate? Draw the circuit and explain its functions.

6 (a) Explain the difference between function and procedure supported by VHDL. Give the necessary examples.
(b) Explain data-flow design elements of VHDL.

7 (a) Give the working principle of analog-multiplexer. Give block diagram of a 16 input analog-multiplexer using CMOS gates and explain how it works.
(b) Draw the logic diagram of 74X174 IC and explain the operation. Develop the VHDL mode for this IC.

8 (a) Explain the operation of edge triggered T flip-flop.
(b) Explain about asynchronous flip flops.

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Code: 9A10504

3

B.Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

LINEAR AND DIGITAL IC APPLICATIONS

(Common to EEE and MCT)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Give the design procedure of a compensating network for an OP-AMP which uses $\pm 10\ \mathrm{V}$ supply voltages. Assume necessary data.
(b) Explain ac analysis of differential amplifier.

2 (a) Describe the principle of operation of precision half wave rectifier with waveforms.
(b) Explain the operation of antilog amplifier using op-amp.

3 (a) Explain how a 555 timer in astable mode can be used for FSK generation.
(b) Design a PLL circuit using 565 IC to get free running frequency = 4.5 KHz, lock range = 2 KHz, capture range = 100 Hz. Assume supply voltages of $\pm 10\ \mathrm{V}$ are available. Show the circuit diagram.

4 (a) What are the parameters that are necessary to define the electrical characteristics of CMOS circuits? Mention the typical values for a CMOS NAND gate.
(b) Compare HC, HCT, VHC and VHCT CMOS logic families with the help of output specifications with $\mathrm{V_{CC}}$ from 4.5 to 5.5 V.

5 (a) Explain the features of the TTL logic family.
(b) Explain the concept and implementation of ECL logic family.

6 (a) Explain the various data types supported by VHDL. Give the necessary examples.
(b) Write a VHDL program to detect prime number of a 8-bit input.

7 (a) Design a 24-bit group ripple adder using 74X283 ICs.
(b) Explain de-multiplexer in detail.

8 (a) Design an 8-bit synchronous binary counter with serial enable control.
(b) Distinguish between latch and flip-flop. Show the logic diagram for both. Explain the operation with the help of function table.

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Code: 9A10504

4

B.Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

LINEAR AND DIGITAL IC APPLICATIONS

(Common to EEE and MCT)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Explain how large open circuit voltage gain of an op-amp can be obtained by using cascading of differential amplifier stages.

(b) Explain the function of various blocks in block diagram of an op-amp.

2 (a) With suitable circuit diagram explain the operation of a triangular wave generator using a comparator and a integrator.

(b) What is an instrumentation amplifier? List any three applications of the instrumentation amplifier.

3 (a) Explain frequency translation and FM detection applications of PLL.

(b) Derive an expression for capture range of PLL.

4 (a) Draw the circuit for CMOS OR logic gate and explain its working clearly.

(b) Which CMOS or TTL logic family has the strongest output driving capability? Explain.

5 (a) Explain how CMOS-TTL interfacing can be achieved. Give the input and output levels of voltages, explain briefly.

(b) Explain low voltage CMOS logic and ECL.

6 (a) Design the logic circuit and write a data - flow style VHDL program for the following function:

$$F(X) = \sum A, B, C, D\ (1, 4, 5, 7, 12, 14, 15) + d\ (3, 11)$$

(b) Explain the use of packages. Give the syntax and structure of a package in VHDL.

7 (a) Write VHDL program for 8-bit comparator circuit. Using this entity write VHDL program for 24-bit comparator.

(b) Design a 4-bit carry look ahead adder using gates.

8 (a) Explain with neat sketch how four bits 1110 are serially entered into the shift register.

(b) With neat circuit diagram explain a master-slave flip-flop and also draw the timing diagram.

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Code: 9AHS701

III B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2013

MANAGEMENT SCIENCE

(Common to EEE & ECC)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 What are the social responsibilities of a manager in twenty first century?

2 Explain the significance and advantages of committee organization.

3 What factors do you keep in mind while developing a suitable plant layout?

4 Explain the concepts of product mix and product line. State the reasons for producing different products by a multi-product firm.

5 (a) Is personnel manager line or staff manager? Support your answer with an example.
(b) Explain in brief how globalization enhanced the need for the HRM function.

6 Write short notes on:
(a) Dummy activity.
(b) Crashing the Network.
(c) Three time estimates of PERT.
(d) Slack and floats.

7 (a) Distinguish between strategic planning, tactical planning and operational planning.
(b) What is SWOT analysis? Explain the process of SWOT analysis.

8 What are the objectives of MRP? Explain how each of these objectives is achieved.

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Code: 9AHS701

2

III B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2013

MANAGEMENT SCIENCE

(Common to EEE & ECC)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 Define management. State the important characteristics of management.

2 Write short notes on:
(a) What is meant by departmentation and decentralization?
(b) Distinguish between formal and informal organization.

3 Explain the concept of SQC. Explain how you can construct control charts for the variables.

4 Define channels of distribution. State its functions.

5 (a) Write a note on recruitment and selection.
(b) Discuss wage and salary administration.

6 (a) Discuss the uses of PERT for planning, scheduling and controlling of projects.
(b) Write a note on Fulkerson's principle.

7 (a) What do you understand by strategic business unit? Discuss its role and relevance in corporate planning.
(b) What do you understand by SWOT analysis?

8 Is re-engineering another fad or does it offers something of lasting value?

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Code: 9AHS701

3

III B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2013

MANAGEMENT SCIENCE

(Common to EEE & ECC)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 Why is management considered as a profession and what factors make it a profession?

2 Discuss the features of line and staff organization and illustrate their suitability.

3 What is work study? Outline the basic procedure involved in work management.

4 Define consumer behaviour. What is its importance in marketing?

5 (a) Differentiate wage and salary. Explain when each of these is admissible with example.
(b) Explore the ways by which human resources can be developed.

6 (a) What is cost slope? What is its significance in project crashing?
(b) Explain how you determine the probability of meeting the scheduled date of completion of a project.

7 What are the factors of external and internal environment to be considered while formulating the strategy?

8 What do you understand by total quality management? How does this concept differ from quality control techniques?

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Code: 9AHS701

4

III B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2013

MANAGEMENT SCIENCE

(Common to EEE & ECC)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 What are the objectives of management? Explain the functions of various management levels.

2 Explain the organization structures with merits & demerits:
(a) Line & Staff.
(b) Functional.
(c) Committee.

3 How does the choice of the building affect lay out decisions?

4 (a) What are the factors that determine the choice of channels of distribution?
(b) Why do manufacturers favour intermediaries?

5 (a) Discuss the major functions of personnel management.
(b) Discuss the concept of job analysis.

6 (a) Explain the utility of PERT and CPM.
(b) What are the various time estimates used in PERT analysis?

7 Distinguish between strategic and operational planning.

8 Explain the process of bench marking. Is it effective in bringing organizational changes?

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