Code: 9A04601

1

III B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2013

DIGITAL COMMUNICATIONS

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Compare and contrast under sampling and over sampling.
(b) What is quantization? Briefly explain about different types of quantization.

2 (a) What is mean by multiplexing? Explain in detail about TDM.
(b) Write about different types of digital multiplexers.
(c) Give the advantages of digital multiplexing.

3 (a) Describe spectral shaping by precoding.
(b) An analog signal is PCM formatted and transmitted using binary waveforms over a channel that is band limited to 100 KHz. Assume that 32 quantization levels are used and that the overall equivalent transfer function is of the raised cosine type with roll off of 0.6. Find:
(i) The maximum bit rate that can be used by this system without introducing ISI.
(ii) The maximum bandwidth of the original analog signal that can be accommodated with these parameters.

4 (a) What are optimal filters? Derive the transfer function of optimum filter.
(b) Discuss the inter symbol interference problem and explain how Nyquist pulse shaping criterion is helpful in eliminating it.

5 (a) Define burst of length (q) and briefly explain about the burst error correcting codes.
(b) Draw and explain a decoder diagram for a (7, 4) majority logic code whose generator polynomial $g(X) = 1 + X + X^3$.

6 Explain the following:
(i) Entropy.
(ii) Information rate.
(iii) Channel Capacity.
(iv) Mutual information.

7 Derive a relation for probability of error and transfer function for optimum filter.

8 (a) Compare M-ary signaling scheme with binary scheme in terms of bandwidth requirements, probability of error and equipment complexity.
(b) With the help of block diagram explain M-ary signaling scheme.

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Code: 9A04601

III B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2013

DIGITAL COMMUNICATIONS

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Explain the principle and working of a quantizer.
(b) Explain in detail about non-uniform quantization.

2 (a) Explain about the T-1 carrier system by presenting the frame structure.
(b) Explain DM system. Also discuss the slope overload distortion and granular noise present in it. Find the signal amplitude for the maximum slope overload error in a DM system. If the step size is 1 V with a repetition period of 1msec. the information signal frequency of 100 Hz.

3 (a) What is the process to suppress (or) eliminate Intersymbol interference and explain in detail?
(b) x(t) is a triangular pulse of 1ms width and 10^{-2} volt height. Assuming the channel noise to be white with a PSD of $\eta = 10^{-8}$ W/Hz, determine the signal to noise ratio at the output of the matched filter.

4 (a) What is the difference between base band transmission and band pass transmission? Distinguish both features.
(b) There are two different principles for shaping the spectrum of a PAM signal. Describe briefly these approaches. What are the central goals and properties (advantages and disadvantages) of these approaches? How does the transmitted signal spectrum depend on the used pulse shape?

5 (a) Explain the operation of convolutional encoders.
(b) Design an encoder for a (7, 4) binary cyclic code generated by $g(X) = 1 + X + X^3$ and explain the operation using the message vector (1 0 1 1).

6 Derive an expression for channel capacity of continuous channel in the presence of white Gaussian noise.

7 (a) Explain DPSK modulation and demodulation with neat block diagrams and differential encoding and decoding table.
(b) In a binary PSK scheme using correlation receiver, the local carrier waveform is $A\cos(\omega_c t + \theta)$ instead of $A\cos(\omega_c t)$ due to poor carrier synchronization.Derive an expression for the probability of error and compute the increase in error probability when $\theta = 15^o$ and A^2T_b/η =10.

8 (a) Draw the block diagram of QPSK demodulator and explain in detail.
(b) Derive a relation for probability of error and band width in QPSK.

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Code: 9A04601

3

III B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2013

DIGITAL COMMUNICATIONS

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Differentiate between ideal sampling and practical sampling.
(b) Derive the transfer function of a gate function required to recover the sampled signal.

2 (a) Discuss different types of noise effects in delta modulation.
(b) Determine the processing gain of a DPCM system with a first order predictor, if the message signal has a normalized auto-correlation function of 0.8 for a lag of one period, assuming that the predictor is designed to minimize the mean –square value of the prediction error.

3 (a) Give the properties of matched filter.
(b) Explain different line codes with the help of waveforms.
(c) Distinguish between pass band and base band transmission.

4 (a) Explain the correlative coding and eye pattern.
(b) Data at a rate of 6 k bit/s is to be transmitted over a leased line of bandwidth 4 kHz by using nyquist criterion pulses. Determine the maximum value of the roll-off factor r that can be used.
(c) For input binary data 1000101 obtain the output of duo-binary encoder and also the output of decoder.

5 (a) What are the properties of linear block codes? Give the mathematical description of linear block codes.
(b) Define syndrome and explain its properties.

6 (a) Write about joint entropy and conditional entropy. Obtain the relation between them.
(b) Consider a Binary Symmetric Channel (BSC). Find the channel capacity for: (i) p = 0.9 and (ii) P = 0.6.

7 (a) Compare digital modulation systems.
(b) Explain the theory of matched filter receiver.

8 Draw the structure of the receiver for an orthogonal wideband FSK signaling scheme and derive a relation for probability of error.

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Code: 9A04601

4

III B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2013

DIGITAL COMMUNICATIONS

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) What is aliasing effect in sampled signal?
(b) How aliasing can be eliminated? Explain with neat diagram.

2 (a) Explain the basic principle of DPCM.
(b) What is meant by bandwidth efficiency of a digital multiplexing system?
(c) Derive an expression for channel noise in delta modulation.

3 (a) Distinguish between pass band and base band transmission.
(b) Derive the power spectral density of NRZ unipolar format.

4 (a) What is a raised-cosine pulse? Describe with the help of diagram.
(b) Compare binary signaling with duo binary signaling.
(c) An analog signal band limited to 6 kHz, is sampled at a rate of 20 x 10^3 sps. The samples are then quantized into 256 levels and coded into M ary amplitude pulses that satisfy Nyquist's criterion with a roll off factor $\rho = 0.3$, if these multi amplitude pulses are to be transmitted over an available channel that has a bandwidth of 32 kHz, determine the minimum acceptable value of M.

5 (a) What are the convolution codes? Explain various methods of decoding convolution codes.
(b) What are burst and random error correcting codes? Explain.

6 (a) What is source encoding? What is its significance? Compare different source encoding algorithms.
(b) Apply the Shannon-Fano coding for the following message ensemble and calculate the efficiency.
$[X] = [x_1, x_2, x_3, x_4, x_5, x_6, x_7,]$.
[P]= [0.4, 0.2, 0.12, 0.08, 0.08, 0.08, 0.04].

7 (a) Derive an expression for probability of error in FSK system.
(b) Show that BPSK is superior to ASK by 3 dB in the average signal power requirement with appropriate mathematical derivations.

8 Explain about M-ary FSK system and derive an expression for probability of error.

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Code: 9A04602

1

III B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2013

MICROPROCESSORS & MICROCONTROLLERS

(Common to EEE, ECE, CSE, EIE & E.Con.E)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Why the lower order address bus is multiplexed with data bus? How they will be de-multiplexed?

(b) Differentiate between maskable and non-maskable interrupts.

2 (a) Write an ALP in 8086 to check the number is prime or not.

(b) Write an ALP in 8086 to convert un packed BCD to packed BCD.

3 (a) Draw the memory write machine cycle in minimum mode and explain the operation in each T state.

(b) Draw and explain the memory write machine cycle in maximum mode.

4 (a) Explain how to interface a stepper motor with 4-step input sequence to 8086 based system with the help of hardware design. Write the instruction sequence to move the stepper motor 10 steps in clockwise and 12 steps in anti-clockwise direction.

(b) Write in detail about stepper motor and actuators and their interface with 8086.

5 (a) What are the applications of 8251? Whether write operation is possible with status word & command word registers.

(b) Distinguish between asynchronous and synchronous data transfer schemes.

6 (a) Draw the block diagram of 8253 and explain about each block in detail.

(b) Explain about control word format and programming of 8253.

7 (a) Explain in brief about programming external hardware interrupts in 8051.

(b) What are the steps involved in programming the 8051 to receive data serially?

8 (a) Explain the importance of each pin in MCS-96 microcontrollers.

(b) Give a short note on 80196 micro controller of MCS-96 family.

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Code: 9A04602

2

III B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2013

MICROPROCESSORS & MICROCONTROLLERS

(Common to EEE, ECE, CSE, EIE & E.Con.E)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Discuss the memory segmentation in 8086 microprocessor.

(b) Briefly explain the architecture of 8086 microprocessor with a neat sketch.

2 Assume that the symbol table starting at location TABLE consists of 100 entries. Each entry has 80 bytes with the first 8 bytes representing the name field and the remaining 72 bytes representing the information field. Write an instruction sequence to search this table for a given name of 8 characters stored in NAME. If the name is found, copy the associated information into INFO, otherwise, fill INFO with null characters.

3 (a) Explain the control pins used in minimum mode operation.

(b) Differentiate minimum and maximum mode of 8086.

4 (a) With neat layout, explain how a microprocessor can be used for data acquisition system using A/D converters and D/A converters.

(b) Explain in detail about the interrupt structure of 8086 microprocessor.

5 (a) What is the significance of SYNC DETECT & BREAK DETECT signals in 8251?

(b) Define command word & status word register of 8251.

6 (a) Draw the pin diagram of 8259 and explain briefly about the function of each pin.

(b) Draw the internal block diagram of 8259 and explain about each block.

7 (a) Write program to load accumulator, DPH & DPL using 8051.

(b) Write short notes on the use of control signals $\overline{WR}$ and $\overline{RD}$.

8 Explain address mapping and memory mapping in detail about MCS-96 micro controllers.

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Code: 9A04602

3

III B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2013

MICROPROCESSORS & MICROCONTROLLERS

(Common to EEE, ECE, CSE, EIE & E.Con.E)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Discuss the various addressing modes of 8086. What are displacement, base and index? What is an effective address or offset?

(b) What are the advantages of the instruction queue in 8086?

2 (a) Write an ALP to separate and count the numbers from positive negative and zero numbers from a given set of 8 bit numbers.

(b) Write an ALP in 8086 to convert packed BCD to unpacked BCD.

3 (a) Explain in brief the need for DMA controller and its working in an 8086 based system.

(b) Differentiate minimum and maximum mode of 8086.

4 (a) Draw the schematic diagram of 8255 PPI and explain different modes of operation of 8255 with example.

(b) Draw the block diagram of 8255 and explain each block.

5 (a) What is parity error, over run error & frame error in 8251? What is hunt mode in 8251?

(b) Explain about USB with necessary example & analysis.

6 (a) Explain the modes of operation of 8253 in detail.

(b) Why do we prefer interrupt driven data transfer than programmed I/O transfer? Show the complete hardware design to resolve the multiple interrupts based on priority.

7 (a) What is assembly language program? What is the function of SWAP? What is debugging?

(b) Write a program to subtract the contents of R1 of Bank 0 from the contents of R0 of Bank 2.

8 (a) Describe about versions and cores of ARM microcontrollers.

(b) Give salient features about ARM microcontrollers.

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Code: 9A04602

4

III B. Tech II Semester (R09) Regular & Supplementary Examinations, April/May 2013

MICROPROCESSORS & MICROCONTROLLERS

(Common to EEE, ECE, CSE, EIE & E.Con.E)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Write an assembly language program that will examine an ASCII string of 100 characters and replace each decimal digit by a %. The character string starts at STRG.

(b) Explain the prefix instruction format of 8086 processor. Discuss how these instructions are useful in string manipulation.

2 (a) Write an ALP in 8086 to multiply two 16 bit numbers and the result is 32 bit.

(b) Write an ALP in 8086 to add two 8 bit ASCII numbers.

3 (a) What are the registers available in 8257? What are their functions?

(b) Draw and discuss the status registers of 8257.

4 (a) Give the relevant hardware and software for interfacing stepper motor to 8086 based system.

(b) Explain A/D converter interface to 8086 micro processor.

5 (a) Define mode word register of 8251 for asynchronous mode.

(b) Define mode word register of 8251 for sync mode.

6 (a) With neat block diagram explain the functions of 8259.

(b) Explain the programming sequence of PIC along with flow chart explain each command word in detail.

7 (a) Write a program to load accumulator A, DPH and DPL with 30 H.

(b) Write short notes on external interrupts of 8051.

8 (a) What is the difference between Interrupt Request (IRQ) and Fast Interrupt Request (FIQ) in ARM? Explain.

(b) Compare the CPSR and SPSR registers formats and their purpose in different modes of ARM processor operations.

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Code: 9A04603

1

B.Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

DIGITAL SIGNAL PROCESSING

(Common to EIE, E.Con.E, ECC & ECE)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 State and Prove following properties DTFT:
(i) Periodicity.
(ii) Time-shifting.
(iii) Multiplication by' n' in time domain.

2 (a) Show that DFS of periodic sequence $x_p(n)$ is periodic with same period.
(b) State and prove duality property of DFS.

3 Write short notes on the following:
(i) Butterfly computation.
(ii) Goertzel algorithm.
(iii) In place computations.
(iv) Bit reversal.

4 Obtain the direct form realization of following system functions with minimum number of multipliers:
(i) $H(z) = (1/2) + (1/4)z^{-1} + (1/4)z^{-2} + (1/2)z^{-3}$.
(ii) $H(z) = [(1-z^{-1}) [(1/2) - (1/4)z^{-1} + (1/2)z^{-2}]]$.

5 (a) Compare the backward and forward difference methods of digital filter approximations.
(b) Convert following analog filter transfer function into digital filter transfer function using backward difference method $H(s) = 1/(s + 2)^2 + 16$.

6 (a) Explain characterization of FIR filters.
(b) Sketch and explain the frequency response of non ideal digital high pass filter.

7 The signal x(n) is up sampled by factor 2, then it is passed through ideal low pass filter with cutoff frequency of F_C and down sampled by factor by 3. Sketch the input and output spectrum for the case (X(F) = tri(4F) with $F_C = 0.15$.

8 (a) Discuss about spectral analysis of sinusoidal signals.
(b) With necessary block diagrams explain about discrete multi tone receiver.

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Code: 9A04603

2

B.Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

DIGITAL SIGNAL PROCESSING

(Common to EIE, E.Con.E, ECC & ECE)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 Discuss the classification discrete systems with the help of examples.

2 Determine the DFT of a sequence x(n) = {1,1,0,0} and check the validity of answer by calculating IDFT.

3 Explain radix 2 DIT-FFT algorithm in detail. Explain how calculations are reduced.

4 If H(z) has zeros at $z_1 = 0.707 + j0.707$, $z_2 = 2$,determine the lowest order degree H(z) that has linear phase. Also realize it in Direct form – II and in Cascade form.

5 (a) Explain the features of Butterworth approximation.
(b) Discuss the location of pole for Butterworth filter.

6 Discuss the type I and II frequency sampling methods of FIR filter design.

7 The signal x(n) is decimated by N to obtain the signal y(n). Sketch X(F) and Y(F) over $-3 \leq F \leq 3$ for the following cases.
(i) x(n) = sinc (0.4 n) N = 2
(ii) X(F) = tri(4 F) N = 2
(iii) X(F) = tri(6 F) N = 3

8 (a) Discuss about spectral analysis of non stationary signals.
(b) Discuss about frequency response of typical band limited channel.

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Code: 9A04603

3

B.Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

DIGITAL SIGNAL PROCESSING

(Common to EIE, E.Con.E, ECC & ECE)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 Check the following systems described with difference equations for linearity, shift invariance, memory and causality

(i) $y(n) - y(n-1) = x(n)$.

(ii) $y(n) - 2^n y(n) = x(n)$.

2 (a) Discuss the relationship of DFT with z-transform.

(b) State and prove periodicity property of DFT.

3 (a) What is the need for FFT?

(b) Find DFT of sequence using DIF-FFT x(n) = {1,1,1,1}.

4 (a) Explain transposed form realization.

(b) Realize following filter system function in cascade form

$H(z) = (1-z^{-1})^3/(1-0.5z^{-1})(1-0.25z^{-1})$.

5 Obtain the analog filter transfer corresponding to filter order of 3 and 4, Consider Butterworth approximation.

6 (a) Explain the type – II frequency sampling method of designing FIR filter.

(b) Explain the process of windowing using illustrations

7 Compare the single stage and two stage realization of decimator with the following specifications. Sampling rate of a signal has to be reduced from 10 KHz to 500 Hz. The decimation filter H(z) has the pass band edge of 150 Hz, stop band edge of 180 Hz, pass band ripple of 0.002 and stop band ripple of 0.001.

8 (a) Explain about STFT.

(b) Discuss the need for signal compression.

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Code: 9A04603

4

B.Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

DIGITAL SIGNAL PROCESSING

(Common to EIE, E.Con.E, ECC & ECE)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 Check for causality and stability of following systems

(i) $y(n) = x(n-1) + x(n) + x(n+1)$.

(ii) $y(n) - 2y(n-1) + y(n-2) = x(n) - x(n-3)$.

2 Given the two sequences

(a) $x_1(n) = 1 \quad 0 \le n \le 3$

(b) $x_2(n) = (-1)^n \quad 0 \le n \le 3$

Find circular convolution of above sequences. Also verify the answer with DFT method.

3 (a) Explain how many complex computations are required to compute N-point DFT.

(b) Find DFT of sequence using DIT-FFT x(n) = {1/2,1/2,0,0}.

4 Discuss the following:

(i) IIR filter structures.

(ii) FIR filter structures.

(iii) Canonic and Non-canonic structures.

5 (a) Discuss the mapping s-domain to z-domain using backward difference method.

(b) Convert following analog filter transfer function into digital filter transfer function using backward difference method $H(s) = 1/(s^2 + 0.9)$.

6 (a) What is the linear phase filter? Give the conditions under which FIR system will have linear phase.

(b) What are the desirable features of windowing functions?

7 Implement a two stage decimator for the following specifications. Sampling rate of the input signal = 21,000 Hz

M = 100

Pass band = 0 to 50 Hz

Transition band = 50 to 70 Hz

Pass band ripple = 0.01

Stop band ripple = 0.002

8 Discuss in detail about time domain operations used in musical sound processing.

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Code: 9A04604

1

B. Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

ELECTRONIC MEASUREMENTS & INSTRUMENTATION

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) What is precision? What are the two characteristics of precision?
(b) Differentiate accuracy and precision.

2 (a) With the help of block diagram explain the functioning of a conventional standard signal generator.
(b) What are the characteristics of signal sources?

3 (a) With the help of a neat sketch, explain the working of a frequency selective wave analyzer.
(b) What is the function of high –Q filter?

4 (a) Define astigmatism, focus and intensity.
(b) State the various applications of an oscilloscope.

5 Describe in details the construction and working of an analog type storage oscilloscope. Explain the principle of secondary emission.

6 (a) Discuss the bridge which is used for the precision measurement of capacitors and their insulating properties. How does the balancing condition help finding the reactance of the unknown component and its dissipation factor?
(b) A bridge has 2000 ohm in one arm and its opposite arm has a capacitor of value 0.5 µF. The arm to the right of resistor arm is having 1000 ohm in shunt with a 0.5 µF. The arm opposite to this arm is connected with the unknown component. Find the value of the component and its dissipation factor.

7 Describe the operation of:
(a) Total radiation pyrometers.
(b) LVDT.
(c) Resistive transducers.

8 Explain the different methods used for producing recorder.

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Code: 9A04604

2

B. Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

ELECTRONIC MEASUREMENTS & INSTRUMENTATION

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Explain the principle used in ohm meters.
(b) Explain with the help of circuit diagram the construction and working of a series type ohm meter.

2 (a) Write about fixed frequency AF oscillator and variable AF oscillator.
(b) Describe with the help of a sketch the basic sine wave generator.

3 (a) Describe with diagram the operation of a digital Fourier analyzer.
(b) Explain in brief the operation of a practical FFT spectrum analyzer.

4 (a) What are the advantages of dual trace oscilloscopes over dual beam CRO?
(b) Explain the operation of delayed sweep CRO.

5 Describe the principle of working and circuit diagram of a digital oscilloscope.

6 Explain in detail about EMI & EMC with suitable examples.

7 (a) Explain the input and output characteristics of the transducers.
(b) Discuss the materials used for potentiometers.

8 Describe components of an analog-data-acquisition system.

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Code: 9A04604

3

B. Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

ELECTRONIC MEASUREMENTS & INSTRUMENTATION

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Explain the construction of a multi range voltmeter.

(b) A moving coil instrument gives a full scale deflection of 10 mA when the potential difference across its terminals is 100 mv. Calculate:

(i) The series resistance for a full scale deflection corresponding to 100 A.

(ii) The series resistance for full scale reading with 1000 v. Calculate the power dissipation in each case.

2 (a) Explain the operating principle of a function generator.

(b) Explain the method of producing sine waves in a function generator.

3 (a) Describe the causes of harmonic distortions.

(b) Explain the basic principle of a digital Fourier analyzer.

4 (a) What are the advantages of negative supply in a CRO?

(b) Compare the dual beam CRO and dual trace CRO.

5 (a) How does the sampling oscilloscope increase the apparent frequency response of an oscilloscope?

(b) What is the relationship between the period of a waveform and its frequency? How is an oscilloscope used to determine frequency?

6 (a) What are the applications of wheat stone bridge? And list out its limitations.

(b) What are the limitations of wheat stone bridge?

7 (a) List three types of temperature transducers and describe the applications of each.

(b) Derive an expression for poissons ratio.

8 What is USB controller? Discuss the architecture of USB controller.

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Code: 9A04604

4

B. Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

ELECTRONIC MEASUREMENTS & INSTRUMENTATION

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) What are the essential requirements of multipliers?
(b) Explain how different full scale voltage ranges may be obtained by the use of individual multiplier resistors or potential divider arrangement.

2 (a) How signal generators are different from self-contained oscillators?
(b) Write brief note about RF signal generators with frequency band limits.

3 (a) Describe with a diagram the operation of a harmonic distortion analyzer using a bridged T- network.
(b) Explain the procedure of measurement of a harmonic distortion analyzer using a bridged T- type.

4 (a) State the standard specification of a sample CRO.
(b) Explain with a diagram how frequency can be measured using a gear wheel method.

5 With a neat block diagram, describe the working of a triggered sweep CRO.

6 (a) Describe the operation of the Wheatstone bridge.
(b) Define the term null as it applies to bridge measurements.

7 (a) What is the operating principle of beta gauge?
(b) What are the various scanning modes of a beta gauge?

8 (a) Explain about I/O address map and PC bus of PC system.
(b) Explain the hard disk features and partitions.

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Code: 9A04605

1

B. Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

VLSI DESIGN

(Common to ECE, EIE & E.Con.E)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) What are the types of major processes used in IC fabrication?
(b) Mention any four advantages of VLSI.
(c) Mention the design flow in VLSI process.

2 (a) Explain clearly about the latch up effects in p well structure with the help of a neat circuit diagrams.
(b) Mention remedies for this effect.

3 Explain lambda based design rules.

4 Derive an equation for the propagation delay from input to output of the pass transistor chain shown in figure.

5 (a) Design logic for an ALU that can perform both logical and arithmetic operations.
(b) Enumerate all the 16 possible functions of a two input ALU.

6 What are the various design options used to implement the CMOS system design explain each in detail?

7 Write a program in VHDL for an 8:1 multiplexer in behavioral and structural style and compare them.

8 (a) Through comparison explain the manufacturing tests and functionality tests.
(b) Mention how many test vectors are required to exhaustively test a combinational circuit with n-inputs and a sequential circuit with n-inputs and m-storage devices respectively.

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Code: 9A04605

2

B. Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

VLSI DESIGN

(Common to ECE, EIE & E.Con.E)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 With neat sketches explain electron lithography process.

2 Explain clearly about different operating regions in nmos transistor with neat diagrams.

3 Draw the CMOS 2 input NAND gate, its physical lay out with its stick diagram.

4 Estimate the total delay when a larger load capacitance is driven by a large inverter gate N which is driven by a small gate N-1 and so on.

5 (a) Provide the design of an 8 × 8 array multiplier.
(b) Explain the working principle of booth multiplier.

6 (a) Write about standard cell based design.
(b) Implement an optimized 3X8 binary decoder using PLA.

7 (a) What are the various styles of writing a program in VHDL? Explain.
(b) Write a program using VHDL in structural style to implement a 3 × 8 binary decoder.

8 (a) What is a fault model? Explain in detail about stuck at fault model.
(b) Explain the terms fault simulation, fault coverage and fault collapsing.

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Code: 9A04605

3

B. Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

VLSI DESIGN

(Common to ECE, EIE & E.Con.E)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Write important characteristics of CMOS.
(b) Why CMOS is preferred over bipolar technology?
(c) Short notes on advanced CMOS fabrication technologies.

2 Mention different non ideal I-V effects and clearly explain about them.

3 (a) What are the effects of scaling on Vt?
(b) Discuss the limits due to sub threshold currents.

4 What is the problem of driving large capacitance load? Explain a method to drive such load.

5 Implement a 4-bit ALU using adder as basic primitive block and explain how the arithmetic and logical operations are performed using adder element.

6 (a) Differentiate between chips with programmable logic structure and chips with programmable interconnect. Give an example for each.
(b) Give a brief description of various methods of programming the programmable array logic (PALs) in CMOS.

7 (a) What is register transfer level (RTL) synthesis?
(b) Explain with an example how RTL descriptions in VHDL capture the attributes of a design.

8 (a) Write about different fault models.
(b) List out all the possible struck at faults for three input NAND gate and thus generate the minimum test vectors that detect all the faults.

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Code: 9A04605

4

B. Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

VLSI DESIGN

(Common to ECE, EIE & E.Con.E)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Explain the evaluation of a VLSI design technology.

(b) Explain clearly about Moore's law.

2 (a) Draw the circuit of nMOS inverter and explain its operation. Draw and explain its transfer characteristics.

(b) Determine the pull-up and pull-down ratio for an nMOS inverter driven by another nMOS inverter.

3 Design a stick diagram for NMOS EX-OR gate.

4 Calculate gate capacitance value of 2 μm technology minimum sized transistor with gate to channel capacitance value of 8×10^4 pF/ohm μm^2.

5 (a) Explain the principle of working of a 4-bit carry-look ahead adder and hence draw the logical schematic used to obtain the generate and propagate signals.

(b) With the help of the logical schematic explain the working of a parity generator.

6 (a) Summarize the difference between reprogrammable gate array designing and programmable interconnect designing.

(b) Give a brief description about full custom design. Justify where full custom design is preferred to semicustom design.

7 Compare the simulation process at various levels of design of chips with respect to complexity of computation, speed and accuracy.

8 (a) With the help of schematic diagram using logical blocks explain the working of BILBO as a test pattern generator.

(b) Discuss about various approaches of design for testability.

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Code: 9A04606

B. Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

MICROWAVE ENGINEERING

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Discuss how the microwave spectrum is categorized into different bands.

(b) What is the need of microwave frequency? Explain different applications of microwaves.

2 Derive equations for maximum energy stored and power dissipated in rectangular cavity.

3 (a) Draw a typical directional coupler and define directivity and coupling coefficient.

(b) Explain how the power is coupled from waveguide with the help of a probe.

4 Show that the scattering matrix for a magic Tee is given by

$$[s] = \frac{1}{\sqrt{2}} \begin{bmatrix} 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 1 & -1 & 0 & 0 \end{bmatrix}$$

5 (a) List out the various advantages of using microwave frequencies for various applications.

(b) With the help of velocity diagram explain principle of two-cavity Klystron amplifier.

6 (a) What is a slow wave structure? Draw any four slow wave structures usable in a traveling wave tube.

(b) Explain the possibility of oscillations in a TWT amplifier. Suggest method to prevent oscillations.

(c) Discuss about the differences between a TWT and a Klystron.

7 (a) What is transferred electron effect? Explain clearly how a GUNN diode is different from a tunnel diode both being a negative resistance devices.

(b) What is parametric amplifier? Explain it as an amplifier and frequency converter.

8 Describe the experiment of reflex klystron characteristics to find the reflex klystron output and frequency characteristics, mode number and transit time.

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Code: 9A04606

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B. Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

MICROWAVE ENGINEERING

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 Derive the expressions for the field components due to TM waves in rectangular wave-guide.

2 (a) Discuss the conductor losses in a micro strip line.

(b) What is the importance of Bessel functions in computing the solutions for fields in circular waveguides?

3 What are the different methods of power coupling to or from a waveguide? Explain probe and loop coupling methods.

4 Explain the importance of S-parameters. Show that the scattering matrix for a section of uniform lossless guide of electrical length $\theta = 2\pi \frac{L}{\lambda_g}$ is

$$[s] = \exp(-j\theta)\begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}.$$

5 (a) List two discriminations between conventional tube and microwave tube. What can be the possible solutions to the limitations of conventional tubes at high frequencies? Which one is the best?

(b) Write short notes on bunching process in a two-cavity klystron amplifier.

6 (a) Write short notes on wave modes.

(b) Mention how a TWT can be converted to an oscillator. Explain the operation of such a device. Why large tuning range, are possible with such a device?

7 (a) Explain the V-I characteristics of a Gunn diode.

(b) List the differences between microwave transistor and TED devices.

8 (a) Describe how an ordinary voltmeter can be calibrated to VSWR directly. What are the drawbacks of such a VSWR meter?

(b) Determine s-parameters of a 10 dB directional coupler of directional coupler of directivity 30 dB. Assuming directivity of coupler loss-less VSWR at each port under matched condition is unity.

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Code: 9A04606

3

B. Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

MICROWAVE ENGINEERING

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Show that a waveguide works like a high pass filter.

(b) A waveguide having dimensions a = 5 cm, b = 2 cm. The signal applied to waveguide is 10 GHz. Determine the modes that are propagating in the waveguide.

2 (a) Why TEM modes are not possible in a hollow rectangular waveguide? Prove it.

(b) Explain in brief about strip line transmission lines.

3 (a) Distinguish between E-plane and H-plane tees and hence discuss the construction and working of a magic Tee.

4 (a) What is an isolator? Explain the principle of working.

(b) Show that the S-matrix of a lossless isolator is given by $[s]=\begin{bmatrix}0 & 0\\ 1 & 0\end{bmatrix}$.

5 Explain the operation of a two cavity klystron amplifier. Derive expressions for bunched beam current and efficiency.

6 (a) Derive the expressions for propagation constant and output power gain of TWT.

(b) In an O-type traveling wave tube, the acceleration voltage is 4000 V and the magnitude of the axial electric field is 4 V/m. The phase velocity on the slow wave structure is 1.10 times the average electron velocity. The operating frequency is 2 GHz. Determine the magnitude of velocity function.

7 Discuss how a decrease in drift velocity with increasing electric field can lead to the formation of a high field domain for microwave generation and amplification.

8 (a) What is spectrum analyzer? List the types of spectrum analyzer. List some application of spectrum analyzer.

(b) Describe a microwave bench.

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Code: 9A04606

4

B. Tech III Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

MICROWAVE ENGINEERING

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 What are the different power losses in rectangular waveguide? Derive expressions for them.

2 Discuss the different losses in micro strip lines and state the reasons for losses.

3 With the help of diagrams, clearly explain the principle and operation of precision variable attenuator.

4 (a) Explain the operation of circulator.
(b) What is Faraday rotation?

5 (a) Describe with the neat sketch the constructional details and principle of operation of a reflex klystron tube. With the help of Applegate diagram illustrate the phenomenon of bunching.
(b) Derive the expressions for bunched beam current and efficiency.

6 (a) Why at microwave frequency we talk of traveling waves with associated powers instead of voltages and currents?
(b) What are slow wave structures? Explain how a helical TWT achieve amplification.

7 (a) Explain the properties of high field domain for microwave generation and amplification.
(b) Explain the rate of growth of space charge layers with the help of necessary expressions.

8 (a) Distinguish between low frequency measurement and microwave measurements.
(b) What are the precautions to be taken while setting up microwave bench for measurement of various parameters? Explain.

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